

# MATTEO D'ADDATO

ELECTRONIC ENGINEER, PHD STUDENT

## PERSONAL INFORMATION

Nationality: Italian

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## EDUCATION

### Ph.D. course in Electronics, Telecommunications, and Information Technologies, University of Bologna

2019 - present (currently in the last year of course)

Research project title: *Ultra-low-power integrated circuits and architectures for Wake-Up Radio receivers*

Supervisors: Prof. Eng. Antonio Gnudi, Prof. Eng. Eleonora Franchi Scarselli

### Master Degree in Electronics Engineering, University of Bologna

Graduated with honors in 2019

Thesis: *Design of an ultra-low-power analog PLL for Wake-Up Radio systems*

Thesis supervisors: Prof. Eng. Antonio Gnudi, Prof. Eng. Eleonora Franchi Scarselli

### Bachelor Degree in Electronics and Telecommunications, University of Bologna

Graduated in 2016

Thesis: *TCAD model for charge transport in integrated circuits packages in humid conditions*

Thesis supervisors: Prof. Eng. Susanna Reggiani, Prof. Eng. Antonio Gnudi

## RESEARCH ACTIVITY

### Research fellow

January 2021 - April 2021

Research project title: *Design and realization of an input matching network for a Wake-Up Radio receiver*

Supervisor: Prof. Eng. Eleonora Franchi Scarselli

### Research fellow

April 2019 - October 2019

Research project title: *Ultra-low-power integrated circuits design in a smart power technology for Internet of Things applications*

Supervisors: Prof. Eng. Antonio Gnudi, Prof. Eng. Eleonora Franchi Scarselli

## MAIN RESEARCH TOPIC

### Wake-Up Radio receivers for Internet of Things applications

Design of ultra-low-power analog and digital integrated circuits in STMicroelectronics 90-nm BCD and CMOS technologies. The research activity has also involved the study of ultra-lightweight cryptographic algorithms to counteract the so-called Denial-of-Sleep attacks in Wake-Up Radio receivers.

## PUBLICATIONS

### Journal papers

- M. D'Addato et al., *A Gated Oscillator Clock and Data Recovery Circuit for Nanowatt Wake-Up and Data Receivers*, Electronics, Mar. 2021. **Rated as Editor's choice article**

### Contribution in conference proceedings

- M. D'Addato et al., *A Gated Oscillator Clock and Data Recovery Circuit for Nanowatt Wake-Up and Data Receivers*, the 52nd annual meeting of the Associazione Società Italiana di Elettronica (SIE), Jul. 2021.
- M. D'Addato et al., *Nanowatt Clock and Data Recovery for Ultra-Low Power Wake-Up Radio Receivers*, Proceedings of the 2020 International Conference on Embedded Wireless Systems and Networks (EWSN '20), Feb. 2020.

## TEACHING ACTIVITY

### Teaching assistance

University of Bologna

June 2021 - present

Course: Digital Systems and Introduction to Computer Architectures

### Co-supervisor for the Bachelor thesis

Pusateri L., *Design of a Printed Circuit Board for custom Wake-Up Radio testing*, University of Bologna, 2020.

Supervisors: Prof. Eng. Elena Gnani, Eng. Matteo D'Addato

### Co-supervisor for the Master thesis

Mazdadi A., *Design of an ultra-lightweight cryptographic unit to counteract Denial-of-Sleep attacks in Wake-Up Radio receivers*, University of Bologna, 2021. Supervisors: Prof. Eng. Eleonora Franchi Scarselli, Eng. Matteo D'Addato

## TECHNICAL AND PROFESSIONAL SKILLS

### Electronics Engineering skills

- Digital integrated circuits: design and functional verification of the HDL code (VHDL and SystemVerilog) using QuestaSim, synthesis using Synopsys Design Compiler and place and route.
- Advanced analog integrated circuits design and custom-layout: design and simulation in Cadence Virtuoso using Spectre/Eldo simulator, system modeling and verification using Verilog-A, reliability simulations (Process, Voltage and Temperature variations, Monte Carlo simulations), layout with Cadence Virtuoso layout suite.
- Design and layout of Printed Circuit Boards.
- Testing and laboratory instrumentation: multimeter, function generator, oscilloscope, network analyzer, spectrum analyzer.

## **Programming languages**

C, Matlab, Python, VHDL, SystemVerilog, Verilog-A

## **Softwares**

Cadence Virtuoso, Modelsim, Keysight Advanced Design System, LTSpice, Microsoft Office

## **Language skills**

Italian (mother tongue) and English (advanced)

## **CONFERENCES ATTENDANCE**

The 52nd Annual Meeting of the Associazione Società Italiana di Elettronica (SIE)

July 7th, 2021 - July 9th, 2021

University of Trieste, Italy

2020 International Conference on Embedded Wireless Systems and Networks (EWSN'20)

February 17th, 2020 - February 19th, 2020

INSA Lyon, France

AWAKE: Wake-Up Radio Technologies for Next Generation Wireless Communications

February 17th, 2020

INSA Lyon, France

## **COURSES ATTENDANCE**

English Course on Academic English Skills

March 1st, 2021 - April 30th, 2021

University of Bologna, Italy

NiPS Winter School 2020

December 15th, 2020 - December 18th, 2020

University of Perugia, Italy

2020 Topics on Microelectronics

September 8th, 2020 - September 10th, 2020

University of Milan-Bicocca, Italy

Elements of Applied Data Security

February 19th, 2020 - June 4th, 2020

University of Bologna, Italy

## **PERSONAL DATA**

I hereby authorize the use of my personal data.