# Luca Valente

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IIS Chip Gallery: authors/lv


## Experience

**Alma Mater Studiorum, Università di Bologna** — Bologna, Italy
Research Fellow, Hardware designer — November 2020–Current

- Contributor to PULP Platform, joint effort between the Integrated Systems Laboratory (IIS) of ETH Zürich and Energy-efficient Embedded Systems (EEES) group of the University of Bologna.
- Winner of the Scholarship: "Hardware-software codesign for parallel architectures targeting machine learning applications", funded by EPI Project.

**Barcelona Supercomputing Center** — Barcelona, Spain
Junior Verification Research Engineer — March 2020–August 2020

- I carried out the work for my Master's Degree Thesis in the Verification Team for the European Processor Initiative (EPI) at the Barcelona Supercomputing Center: it consisted in developing an Assertion-based Functional Verification Plan for several submodules of a Vector Processing Unit. The VPU under development works as a co-processor of a RISC-V scalar core, to enable the support for the 0.7.1 RISC-V Vector Extension.

## Education

**Università di Bologna** — Bologna, Ita
Ph.D. in Electronic Engineering, Advisor: Luca Benini — November 2020–Current

**Politecnico di Torino** — Torino, Ita
M.S. in Electronic Engineering, Final Grade: 110/110 — October 2018–October 2020

- Major: Electronic Systems.
- Thesis: "A Vector Processing Unit implementation for RISC-V Vector Extension: Functional Verification and Assertions on submodules" at Barcelona Supercomputing Center. Available here.

**Universitat Politecnica de Catalunya** — Barcelona, Spain
Erasmus Master Student in Electronic Engineering, Avg. Grade: 8.6/10 — September 2019–August 2020

- Focus of the Erasmus Courses: Deep Learning, Audio and Video Processing.

**Università di Bologna** — Bologna, Ita
B.S. in Electronic and Telecommunication Engineering, Final Grade: 105/110 — October 2015–July 2018

- Thesis: "Studying and Modelling of Power Control Logic in IBM OpenPOWER Processor for HPC"

**Liceo Scientifico** — Forlì, Ita
High School, Final Grade: 91/100 — September 2010–July 2015

## Publications


1. S. Preatto; A. Giannini; L. Valente; G. Masera and M. Martina. *"Optimized VLSI Architecture of HEVC Fractional Pixel Interpolators with Approximate Computing"*, in J. Low Power Electron. Appl. 2020, 10(3), 24, https://doi.org/10.3390/jlpea10030024

## Volunteer Experience

**Scout Leader** Forlì, Ita
AGESCI 2015–2018

## Languages

- **Italian:** Mother Tongue
- **English:** C1, IELTS Certification:7.5
  - July 2018, Credential ID: 18IT004542VALL010A
- **Spanish:** B1, OLS Erasmus Test

## Academic Projects

- **Tapeout of Darkside**
  Università di Bologna May 2021–July 2021
  - Darkside is a PULP based chip. It features 4 different hardware accelerators and targets Machine Learning workloads. It also provides a 32kB macro-memory from EPFL, able to perform both conventional and in-memory computing operations.
- **Tapeout of Echoes**
  Università di Bologna April 2021–July 2021
  - Echoes is a PULPissimo based chip. It uses the new CV32E40P from OpenHW group as Fabric Controller (FC). It is designed for audio-processing applications. It supports I2S protocol and features an FFT accelerator.
- **MobileNetV2 inference on Pulp System on FPGA**
  Università di Bologna November 2020–February 2021
  - Bringing the MobileNetV2 automatically generated by Dory on Pulp on FPGA (ZCU102 by Xilinx). Particular focus on functional validation and update of the drivers for the module used to communicate with Flash and Ram memories.
- **Audio Classification of Urban Sounds with DL**
  Universitat Politecnica de Catalunya October 2019–December 2019
  - We developed a CNN able to label 23 different sources of urban sounds from raw audio data of 10 seconds. Our goal was to assess the impact of the number of parameters and of the sample frequency o the performance of the system.
- **Deep Learning on MNIST Dataset**
  Universitat Politecnica de Catalunya December 2019
  - Implementation of an Autoencoder, a GAN and a Classifier on MNIST Dataset.

## Skills

- **Programming:** System Verilog, Python, C, Matlab, SVA, VHDL, Bash, TCL, Gitlab CI.
- **Computer SW:** Quartus, Modelsim, Cadence, Virtuoso, Innovus, Synopsis, Simulink, Questasim, QuestaCDC.