Curriculum Vitæ et Studiorum

Name	Francesco Barchi
Citizenship	Italian
Affiliation	Università di Bologna Dipartimento di Ingegneria dell'Energia Elettrica e dell'Informazione "Guglielmo Marconi"
Address	Viale del Risorgimento 2, 40136 Bologna (BO) - Italy
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Short Bio

Since 2016, Francesco Barchi has published (international, peer-reviewed) 7 journal papers and 12 conference papers. Publications include IEEE and ACM journals. His h-index is 6 (from Google Scholar, on November 1st, 2022), for a total of 135 citations. He is currently a postdoctoral researcher at the DEI department of the University of Bologna.

He started his scientific research activity in October 2015 at Politecnico di Torino, focusing on neuromorphic architectures and programming models for multicore architectures.

During his PhD (2016-2019), Francesco Barchi has expanded these research topics on embedded multicore and many-core platforms. He built his knowledge in partitioning and placement of Spiking Neural Networks on neuromorphic devices, Deep Learning for source code analysis, and middleware development for Globally Asynchronous Locally Synchronous architectures. In 2019 Francesco Barchi was a PhD visiting student at the D-ITET department at ETH Zurich studying domain-specific compilers for deep neural networks. During his stay at Politecnico di Torino, he was involved in Human Brain Project, a flagship European research project. He had the chance to gain a more in-depth understanding of neuromorphic devices, including SpiNNaker architecture. During those years, he started working on research activities involving brain-inspired architectures and machine learning applied to compiler optimizations, expanding his expertise in programming Manycore and Heterogeneous Architectures. During his postdoctoral research activities at UNIBO (2020), he was involved in the INSIST Project, where he gained the opportunity to learn advanced knowledge in vertical applications of embedded architectures involving Structural Health Monitoring and Cyber-Physical Systems. In 2021 he was involved in a funded research project in collaboration with Technology Innovation Institute (TII), New York University (NYU) and Università di Bologna (UNIBO). He supported the scientific and technical coordination of the project, whose topics focus on UAV Perception, Navigation, Communication and Swarm. In the same year, he was responsible for UNIBO technical activities for two other research-funded projects with the Technology Innovation Institute (TII) to develop a secure SoC based on RISC-V processor architecture for UAVs and micro UAVs.

Currently, Francesco Barchi is involved in the research activities of the ECS group at the University of Bologna, where he is leading the technical development of ECS group-funded projects, and he is supervising the technical activities of three PhDs students, one research assistant and several master thesis students.

Contents

Positions and Education

TRAINING AND RESEARCH ACTIVITIES

2019/11 - present

Postdoctoral fellow at the Department of Electrical, Electronic and Information Engineering "Guglielmo Marconi" (DEI), Università di Bologna, Italy. 3-year research activity.
(Reference *Prof. Andrea Acquaviva*).

2019/4 - 2019/10

Visiting researcher at the Department of Information Technology and Electrical Engineering, Eidgenössische Technische Hochschule Zürich (ETH), Switzerland. 6-month research activity.
(Reference *Prof. Luca Benini*).

2015/10 - 2016/10

Research assistant at the Department of Control and Computer Engineering (DAUIN), Politecnico di Torino, Italy. 1-year research activity.
(Reference *Prof. Enrico Macii*).

SPECIFIC PROFESSIONAL EXPERIENCES

2013/12/2 - 2013/12/4

Corporate Venturing "Italia Lab", Idea Generation & Evaluation at Microsoft and Consortium of Companies ELIS (CONSEL), Roma, Italy.
(Reference *ELIS Consortium*).

2013/8/29 - 2013/9/03

Talent Program "School Of Future Leaders" at Consortium of Companies ELIS (CONSEL), Roma, Italy.
(Reference *ELIS Consortium*).

2012/09

Software Developer for GAMUT. Software development for statistical surveys on dangerous goods transit in the Pont-Saint-Martin highway, Torino, Italy. (Reference *Dr. Emanuele Bena*)

2012/03 - 2012/08

Intern in GAMUT, for development and optimization of a software tool for Multichannel Analysis of Surface Waves, Torino, Italy. (Reference *Dr. Emanuele Bena*)

EDUCATION

- PhD in Computer and Control Engineering at the Department of Control and Computer Engineering (DAUIN), Politecnico di Torino. A 3-year course of study and research activity. October 2, 2020
  Thesis Title: *Many-core and Heterogeneous Architectures: Programming models and Compilation Toolchains*
  Advisor: *Prof. Enrico Macii*
- M.Sc. in Computer Engineering at the Department of Control and Computer Engineering (DAUIN), Politecnico di Torino. A 2-year course of study. July 31, 2015
  Thesis title: *Software Development for Optimization of Spiking Neural Network Simulations on Multi-processor Neuromorphic Hardware*,
  Advisor: *Prof. Andrea Acquaviva*
- B.Sc. in Computer Engineering at the Department of Control and Computer Engineering (DAUIN), Politecnico di Torino. A 3-year course of study. October 19, 2012
  Thesis Title: *Development and Optimization of a Software Tool for the Analysis of MASW (Multichannel Analysis of Surface Waves) Inspection Data*. Advisor: *Prof. Edgar Ernesto Sanchez Sanchez*

Prices and academic rewards

AW.1. Ph.D, Quality Awards 2019 (3rd Year), DAUIN, Politecnico di Torino

AW.2. Ph.D, Quality Awards 2018 (1st and 2nd Year), DAUIN, Politecnico di Torino

AW.3. IEEE 1st New Generation of Circuits and Systems Conference "Bronze Leaf Award" for the contribution "An Efficient MPI Implementation for Multi-Core Neuromorphic Platforms".

CONTRIBUTION TO CONFERENCE AND JOURNAL ORGANIZATION

- Program Committee in The Second International Workshop on Artificial Intelligence methods for Smart Cities (AISC 2022) as a part of the EUSPN International Conference. October 26-28, 2022. Leuven, Belgium.
- Program Committee member in IEEE International Conference on Omni-layer Intelligent systems (COINS-22) August 1-3, 2022. Barcelona, Spain.
- Program Committee member in ACM 19th International Conference on Computing Frontiers (CF-22) May 17-19, 2022. Torino, Italy.
- Program Committee member in IEEE 13th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSOC-19) October 1-4, 2019. Singapore.
- Program Committee member in The embedded operating system workshop (EWiLi2018) September 30 - October 5, 2018. Torino, Italy.
- Guest Editor in MDPI Journal of Low Power Electronics and Applications (JLPEA) - Special Issue "Advances in Programming Parallel and Heterogeneous Computing for Cyber-Physical Systems".

Contribution to National and International Research Projects

EdgeAI Work Package Leader (WP2) in "EdgeAI", HORIZON-JTI-KDT-2021. F.B. is in charge of coordinating with partners and WP participants. The project goal is to make available new designs and optimized versions of DNN and neuromorphic accelerators for edge platforms tailored to industrial use cases. Then, apply the compiler-assisted methodology to the allocation of AI tasks on edge and consider industrially relevant non-functional metrics for task allocation optimisation.

HBP Technical coordinator and Technical contributor in "Human Brain Project" (HBP), H2020-EU.1.2. - Excellent Science - Future and Emerging Technologies (FET) Flagship project, SGA-RIA. 2013-2017, 2016-2018 (SGA1), 2018-2020 (SGA2). F.B. was in charge of coordinating with partners and developing solutions for optimising the interconnection of the processors that are part of the SpiNNaker neuromorphic hardware. Speaker at the following project meetings:

March 6-7, 2019 HBP-SP9 Meeting, Graz, AT

February 5-8, 2019 3rd HBP Student Conference, Gand, BE

March 8-9, 2018 HBP-SP9 Meeting, Lausanne, CH

October 16-18, 2018 6th Annual HBP Summit, Maastricht, NL.

October 18-20, 2017 5th Annual HBP Summit, Glasgow, GB.

July 11-12, 2016 HBP-SP9 Meeting, Heidelberg, DE.

INSIST Technical coordinator and technical contributor in "Sistema di monitoraggio INtelligente per la Sicurezza delle InfraStrutture urbane" (INSIST), PON R&I, 2014-2020. F.B. was in charge of internal coordination and developing solutions for the use of MEMS sensors in the structural health monitoring (SHM) field, and developing demonstrators and comparison systems with piezoelectric sensors.

EPI Technical contributor in "European Processor Initiative" (EPI), H2020-EU.2.1.1. Industrial Leadership, SGA-RIA. 2018-2021.

ARROWHEAD Technical contributor in ARROWHEAD, FP7-JTI-CP-ARTEMIS, 2013-2017.

Contribution to Industrial Research Projects

TII-ARRC Technical coordinator in "Develops a state-of-the-art autonomous vehicles platform for aerial drones (UAV) and micro-drones (MAV) swarms" - Commercial and research project with Università di Bologna (UNIBO), New York University (NYU), and Technology Innovation Institute (TII).

TII-SSRC1 Technical coordinator in "Develop a state-of-the-art System on Chip (SoC) for autonomous UAV"- Commercial and research project with Technology Innovation Institute (TII) and Università di Bologna (UNIBO).

TII-SSRC2 Proposal writer and technical coordinator in "Develop a zero-trust solution for System on Chip (SoC) in the field of autonomous UAV" - Commercial and research project with Technology Innovation Institute (TII) and Università di Bologna (UNIBO).

RESEARCH GROUP COORDINATION AND ORGANIZATION

PhDs students and Research assistant Supervision/Co-Advisor

- (2020-ongoing) Two PhD students at Università di Bologna
- (2021-ongoing) One PhD student at Università di Bologna with Telecom Italia
- (2022-ongoing) Three PhD students at Università di Bologna

Graduate Students Supervision/Co-Advisor

- Master Thesis (2) supervisor at Università di Bologna. Italy.
- Master Thesis (6) supervisor at Politecnico di Torino, Italy.

SPEAKER AT INTERNATIONAL CONFERENCES AND PROJECT MEETINGS

- International Conference. 56th ACM/IEEE Design Automation Conference (DAC). June 2-6, 2019. Las Vegas, Nevada (USA).
- Project Meeting. HBP-SP9 Meeting. March 6-7, 2019. Graz, (AT).
- International Conference. 3rd HBP Student Conference. February 5-8, 2019. Gand, (BE).
- Project Meeting. 6th Annual HBP Summit. October 16-18, 2018. Maastricht, NL.
- International Conference. IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC). October 8-10, 2018. Verona, Italy.
- International Conference. 14th ACM/IEEE Embedded System Week (ESWEEK) - International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES). September 30 - October 5, 2018. Torino, Italy.
- Project Meeting. HBP-SP9 Meeting. March 8-9, 2018. Lausanne, CH
- Project Meeting. 5th Annual HBP Summit. October 18-20, 2017. Glasgow, GB.
- International Conference. 1st IEEE New Generation of CAS (NGCAS). September 7-9, 2017. Genova, Italy.
- Summer School. 4th HBP School - Future Computing June 12-18, 2017. Obergurgl University Center, (AT).
- International Conference. IEEE 10th International Symposium on Embedded Multicore/Many-Core Systems-on-Chip, MCSoC. September 21-23, 2016. Lyon, France.
- Project Meeting. HBP-SP9 Meeting. July 11-12, 2016. Heidelberg, DE.

Teaching Activities

PROFESSOR ON CONTRACT

- 2022-2023, Laboratorio di Informatica P1-LU, Mechatronic Engineering
  Università di Bologna. 3 CFU.
- 2022-2023, Laboratorio di Informatica P1-IM, Mechatronic Engineering
  Università di Bologna. 3 CFU.
- 2021-2022, Laboratorio di Informatica P1-IM, Mechatronic Engineering
  Università di Bologna. 3 CFU.

TEACHING ASSISTANT

- 2020-2021, Fondamenti di Informatica P1, Mechatronic Engineering
  Università di Bologna. 6 CFU.
- 2020-2021, Fondamenti di Informatica T, Automation Engineering
  Università di Bologna. 9 CFU.
- 2018-2019, Informatica, All Undergraduate Engineering classes
  Politecnico di Torino. 6 CFU.
- 2017-2018, Informatica, All Undergraduate Engineering classes
  Politecnico di Torino. 6 CFU.
- 2016-2017, Informatica, All Undergraduate Engineering classes
  Politecnico di Torino. 6 CFU.

ACADEMIC TUTOR

- 2020-2021, Fondamenti di Informatica P1, Mechatronic Engineering
  Università di Bologna. 6 CFU.

OTHER TEACHING ACTIVITIES

- 2015-2016, PhD lecturer 3h course “Methods and tools for bioinformatics”
  Politecnico di Torino. (Reference Prof. Andrea Acquaviva)

Research Interests

My main research focus is on cyber-physical systems and embedded devices. In particular, I am interested in: (i) Many-core architectures and globally asynchronous locally synchronous (GALS) system. In this domain, I am interested in optimization methodologies, algorithms and strategies suitable to make these architectures capable of operating in a different computing paradigm (e.g. neuromorphic devices). (ii) Middleware for communication and programming models for many-core architectures. Novel architectures expose innovative ways to manage communication-intensive applications, develop a middleware capable of exploiting these capabilities is a necessary building block to provide complex programming models API. (iii) Machine intelligence applied to source code. Cyber-physical systems and modern embedded devices present a high heterogeneity

in computing components. The mapping procedure between tasks and compute units is not always straightforward, and novel deep-learning algorithms can give some insight into how to solve the problem. (iv) Sensor Networks and embedded devices for on-edge Structural Health Monitoring (SHM). Ultra-low-power embedded devices and deep-learning solutions can help move the anomaly-detection computation near the sensor node to save the energy otherwise used for transmissions. (v) Spiking neural networks usage in CPS. The new generation of neural networks, modelled as dynamical systems, can be used to implement ultra-low power solutions in cyber-physical systems exploiting their temporal domain and communication sparsity. Finally, I am interested in studying how novel methodologies for training SNN through Reinforce Learning can be used in CPS and real-world scenarios.

(I) MANY-CORE AND GALS ARCHITECTURES

For these architectures, the principal investigation theme is resource optimization (e.g. processing, communication, memory, power). These technologies were also explored in-depth in the neuromorphic community. In the last decade, this novel computation paradigm, inspired by biological brain functioning, has been implemented in different hardware architectures: TrueNorth (IBM), BrainScaleS (Universität Heidelberg), SpiNNaker (The University of Manchester), Loihi (Intel).

My experience in this research area was driven by the HBP project, more specifically in working on S.B. Furber's architecture SpiNNaker, a many-core GALS architecture designed as neuromorphic hardware. The contribution in this field has been the creation of tools and methodologies for optimising the resource allocation of computing elements to alleviate the network-on-chip (NoC) and the whole board inter-connectivity pressure. This has been done with the creation of a "software interposer" between configuration software layers in order to adapt the computational graph to the architecture shape [JR.7]. In this field, I have studied scalable algorithms for graph partitioning as well as task placement [BC.1], [IC.6] and performed a whole interconnect profiling procedure [IC.12].

(II) MIDDLEWARE FOR COMMUNICATION AND PROGRAMMING MODELS ARCHITECTURES

Several research teams inside the neuromorphic community have designed platforms and programming models for facilitating the simulation of brain-inspired neural networks performed by neuroscientists. The exploitation of these novel architectures, specifically their interconnect and massively parallelism, is not fully exploited for the lack of a specialized communication middleware capable of exposing the right functionality to developers.

The contribution in this field has been the exploration of how to implement consolidated programming models for these emerging architectures, such as neuromorphic accelerators and heterogeneous architectures. This activity has driven the implementation of a middleware to exploit a massive many-core communication in different manners, from the implementation of MPI support [IC.9], bronze-leaf award-winning at NGCAS, to the implementation of better device configurator and real-time interoperability with neural network simulations [JR.5], [IC.11]. This contribution paved the way for the usage of neuromorphic devices based on many-core architectures also in new domains such as DNA sequence matching algorithm [JR.6].

(III) MACHINE INTELLIGENCE APPLIED TO SOURCE CODE

To cope with the increasing complexity of digital systems programming, deep learning techniques have recently been proposed to enhance software deployment by analysing source code for different purposes, ranging from performance and energy improvement to debugging and security assessment. As embedded platforms for Cyber-Physical Systems are characterised by increasing heterogeneity and parallelism, one of the most challenging and specific problems is efficiently allocating computational kernels to available hardware resources. In this field, deep learning applied to source code can be a key enabler in facing this complexity.

My contribution in this field has been the study to perform a direct analysis of LLVM intermediate representation using deep learning algorithms [JR.1]. In [IC.5], I propose a preprocessing pipeline to analyze a code

fragment after an LLVM compilation step using an LSTM network directly in LLVM-IR. An improved solution is proposed in [JR.3] using a different network model to obtain a 4x-7x shorter training time. In [JR.2], a more specific analysis was conducted on the contribution of auxiliaries information about code execution (e.g. data features) and a Siamese Network was proposed to obtain state-of-art results. Analysis based on traditional machine-learning instruments like decision trees has been successfully applied on ultra-low-power multicore devices (PULP) in order to identify the best efficient parallelism in terms of energy saving [IC.3].

(IV) Sensor Networks and embedded devices for on-edge SHM

Civil infrastructures degrade over time due to use, accidental events, or harsh environmental conditions. Considering the constant growth of large-scale civil infrastructures built worldwide, a cost-effective solution for continuous observation of structural integrity is becoming essential for their maintenance.

Structural Health Monitoring (SHM) techniques assess the structural state and determine the required maintenance and repair. Accelerometers represent the core component of these monitoring systems. MEMS (Micro-Electro-Mechanical Systems) capacitive accelerometers, with their extremely low-cost and low power, permit to design and deploy a steady measurement infrastructure for continuous monitoring to scale up to hundreds of measurement points for a single building. A comparison with piezo accelerometers and a characterization of representative MEMS devices are needed before exploring deep-learning solutions to move the anomaly-detection computation near the sensor node and unveil these devices' potential.

My contribution was the realization of a prototyping board in the framework of INSIST project [IC.2]. The board is equipped with a pair of digital MEMS configured, one in High-Performance and the other in Low-Power mode, thus simultaneously measuring the same stimuli. Comparisons are carried out using a piezoelectric accelerometer as a reference. The characterization is performed in both time and frequency domains focusing on SHM application-specific metrics and using a laboratory set-up and a real-world infrastructure (26 meters long reinforced concrete beam taken from a highway bridge). Investigating the metrological properties of digital MEMS configured in two working modes, Low-Power (LP) and High-Performance (HP), allows trading sensor power consumption for measurement accuracy.

(V) Spiking neural networks usage in CPS and SHM

Recent research in the SHM field demonstrated the effectiveness of low-cost MEMS accelerometers in monitoring buildings' vibrations and the effectiveness of neural networks when used to analyse these data streams. A novel SHM approach can be using Spiking Neural Networks (SNNs) applied to MEMS data to detect infrastructural damages or, more generally, identify anomalies. SNNs are brain-inspired network models that are promising as being more compact and potentially energy-efficient than traditional networks. In particular, Long Short-Term SNN (LSNN) are very effective in analysing data streams but require a non-trivial learning process.

To this purpose, my contribution was the feasibility study of LSNNs for anomaly detection in SHM. I compared the LSNN accuracy with alternative artificial neural network (ANN) models [IC.4], demonstrating that SNN can effectively discriminate whether a structure is in a healthy or damaged condition with an accuracy level similar to ANN. For this purpose, I exploited a state-of-the-art fast training algorithm approximating the Back Propagation Through Time (BPTT). I also show that inference times are compliant with real-time SHM requirements and provide a possible implementation in an embedded device measuring power and energy consumption of the system [JR.4].

Publication List

International journals (# 7)
International books and book chapters (# 1)
International conferences and workshops (# 12)

REFEREED INTERNATIONAL JOURNALS

JR.1. Francesco Barchi, Emanuele Parisi, Andrea Bartolini, Andrea Acquaviva. 2021, Deep Learning Approaches to Source Code Analysis for Optimization of Heterogeneous Systems: Recent Results, Challenges and Opportunities. In Journal of Low Power Electronics and Applications, ISSN:2079-9268. (Scimago Q2 in Engineering - Electrical and Electronic Engineering).
Published by MDPI. DOI:10.3390/jlpea12030037.

JR.2. Emanuele Parisi, Francesco Barchi, Andrea Bartolini, Andrea Acquaviva. 2021. Making the Most of Scarce Input Data in Deep Learning-based Source Code Classification for Heterogeneous Device Mapping. In IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, ISSN:0278-0070. (Scimago Q1 Computer Science - Computer Graphics) (Scimago Q2 Computer Science - Computer Aided Design Software) (Scimago Q1 Engineering - Electrical and Electronic Engineering)
Published by IEEE. DOI:10.1109/TCAD.2021.3114617.

JR.3. Francesco Barchi, Emanuele Parisi, Gianvito Urgese, Elisa Ficarra, Andrea Acquaviva. 2021. Exploration of Convolutional Neural Network models for source code classification. In Engineering Applications of Artificial Intelligence, ISSN:0952-1976. (Scimago Q1 Computer Science - Artificial Intelligence), (Scimago Q1 Engineering - Control and Systems Engineering) (Scimago Q1 Engineering - Electrical and Electronic Engineering)
Published by Elsevier. DOI:10.1016/j.engappai.2020.104075.

JR.4. Francesco Barchi, Luca Zanatta, Emanuele Parisi, Alessio Burrello, Davide Brunelli, Andrea Bartolini, Andrea Acquaviva. 2021. Spiking neural network-based near-sensor computing for damage detection in structural health monitoring. In Future Internet, EISSN:1999-5903.
Published by MDPI. DOI:10.3390/fi13080219.

JR.5. Francesco Barchi, Gianvito Urgese, Alessandro Siino, Santa Di Cataldo, Enrico Macii, Andrea Acquaviva. 2019. Flexible on-line reconfiguration of multi-core neuromorphic platforms. In IEEE Transactions on Emerging Topics in Computing, ISSN:2168-6750.
Published by IEEE. DOI:10.1109/TETC.2019.2908079.

JR.6. Gianvito Urgese, Francesco Barchi, Emanuele Parisi, Evelina Forno, Andrea Acquaviva, Enrico Macii. 2019. Benchmarking a many-core neuromorphic platform with an MPI-based DNA sequence matching algorithm. In Electronics, ISSN:2079-9292.
Published by MDPI. DOI:10.3390/electronics8111342.

JR.7. Gianvito Urgese, Francesco Barchi, Enrico Macii, Andrea Acquaviva. 2016. Optimizing Network Traffic for Spiking Neural Network Simulations on Densely Interconnected Many-Core Neuromorphic Platforms. In IEEE Transactions on Emerging Topics in Computing, ISSN:2168-6750.
Published by IEEE. DOI:10.1109/TETC.2016.2579605.

INTERNATIONAL BOOKS AND BOOK CHAPTERS

BC.1. Francesco Barchi, Gianvito Urgese, Enrico Macii, Andrea Acquaviva. 2018. Mapping Spiking Neural Networks on Multi-core Neuromorphic Platforms: Problem Formulation and Performance

Analysis. In IFIP Advances in Information and Communication Technology, ISSN:1868-4238. Published by Springer. DOI:10.1007/978-3-030-23425-6_9.

REFEREED INTERNATIONAL CONFERENCES AND WORKSHOPS

IC.1. Nicola Elia, Francesco Barchi, Emanuele Parisi, Livio Pompianu, Salvatore Carta, Andrea Bartolini, Andrea Acquaviva. 2022. Smart Contracts for Certified and Sustainable Safety-Critical Continuous Monitoring Applications In Springer Lecture Notes in Computer Science, Advances in Databases and Information Systems - Proceedings, Conference date: September 5-8, 2022. Torino, Italy. ISBN:978-3-031-15740-0. DOI:10.1007/978-3-031-15740-0_27

IC.2. Emanuele Parisi, Amirhossein Moallemi, Francesco Barchi, Andrea Bartolini, Davide Brunelli, Nicola Buratti, Andrea Acquaviva. 2022. Time and Frequency Domain Assessment of Low-Power MEMS Accelerometers for Structural Health Monitoring In IEEE International Workshop on Metrology for Industry 4.0 and IoT, MetroInd 4.0 and IoT - Proceedings, Conference date: June 7-9, 2022. Trento, Italy. DOI:10.1109/MetroInd4.0IoT54413.2022.9831707.

IC.3. Emanuele Parisi, Francesco Barchi, Andrea Bartolini, Giuseppe Tagliavini, Andrea Acquaviva. 2021. Source Code Classification for Energy Efficiency in Parallel Ultra Low-Power Microcontrollers. In Design, Automation and Test in Europe Conference and Exhibition, DATE - Proceedings, Conference date: February 1-5, 2021. Virtual edition. ISSN:1530-1591, ISBN:978-3-9819263-5-4. DOI:10.23919/DATE51398.2021.9474085.

IC.4. Luca Zanatta, Francesco Barchi, Alessio Burrello, Andrea Bartolini, Davide Brunelli, Andrea Acquaviva. 2021. Damage detection in structural health monitoring with spiking neural networks. In IEEE International Workshop on Metrology for Industry 4.0 and IoT, MetroInd 4.0 and IoT 2021 - Proceedings, Conference date: June 7-9, 2021. Virtual edition. ISBN:978-1-6654-1980-2. DOI:10.1109/MetroInd4.0IoT51437.2021.9488476.

IC.5. Francesco Barchi, Gianvito Urgese, Enrico Macii, Andrea Acquaviva. 2019. Code Mapping in Heterogeneous Platforms Using Deep Learning and LLVM-IR. In 56th ACM/IEEE Design Automation Conference (DAC) - Proceedings, Conference date: June 2-6, 2019. Las Vegas, Nevada (USA). ISBN:978-1-4503-6725-7. DOI:10.1145/3316781.3317789.

IC.6. Francesco Barchi, Gianvito Urgese, Andrea Acquaviva, Enrico Macii. 2018. Directed graph placement for SNN simulation into a multi-core GALS architecture. In IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) - Proceedings, Conference date: October 8-10, 2018. Verona, Italy. ISBN:978-1-5386-4756-1. DOI:10.1109/VLSI-SoC.2018.8644782.

IC.7. Francesco Barchi, Gianvito Urgese, Enrico Macii, Andrea Acquaviva. 2018. Impact of Graph Partitioning on SNN Placement for a Multi-Core Neuromorphic Architecture - Work-in-Progress. In 14th ACM/IEEE Embedded System Week, International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES) - Proceedings, Conference date: September 30 - October 5, 2018. Torino, Italy. ISBN:978-153865564-1. DOI:10.1109/CASES.2018.8516831.

IC.8. Gianvito Urgese, Luca Peres, Francesco Barchi, Enrico Macii, Andrea Acquaviva. 2018. Multiple alignment of packet sequences for efficient communication in a many-core neuromorphic system: Work-in-progress In 14th ACM/IEEE Embedded System Week, International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES) - Proceedings, Conference date: September 30 - October 5, 2018. Torino, Italy. ISBN:978-153865564-1. DOI:10.1109/CASES.2018.8516870.

IC.9. Francesco Barchi, Gianvito Urgese, Enrico Macii, Andrea Acquaviva. 2017. An Efficient MPI Implementation for Multi-Core Neuromorphic Platforms. In 1st IEEE New Generation of CAS (NGCAS) - Proceedings, Conference date: September 7-9, 2017. Genova, Italy. ISBN:978-1-5090-6447-2 DOI:10.1109/NGCAS.2017.31.

IC.10. Ramakrishna Venkata Nittala, Francesco Barchi, Gianvito Urgese, Andrea Acquaviva. 2016. Toolchain integration of runtime variability and aging awareness in multicore platforms. In IEEE Forum on Specification and Design Languages (FDL) - Proceedings, Conference date: September 14-16, 2016. Bremen, Germany. ISBN:979-10-92279-17-7 DOI:10.1109/FDL.2016.7880384.

IC.11. Alessandro Siino, Francesco Barchi, Sergio Davies, Gianvito Urgese, Andrea Acquaviva. 2016. Data and Commands Communication Protocol for Neuromorphic Platform Configuration. In IEEE 10th International Symposium on Embedded Multicore/Many-Core Systems-on-Chip, MCSoC - Proceedings, Conference date: Sep 21-23, 2016. Lyon, France. ISBN:9781509035304, DOI:10.1109/MCSoC.2016.41.

IC.12. Gianvito Urgese, Francesco Barchi, Enrico Macii. 2015. Top-Down Profiling of Application Specific Many-core Neuromorphic Platforms. In IEEE 9th International Symposium on Embedded Multicore/Many-Core Systems-on-Chip, MCSoC - Proceedings, Conference date: Sep 23-25, 2015. Torino, Italy. ISBN:978-1-4799-8670-5 DOI:10.1109/MCSoC.2015.43.

Date 04/03/2023