Davide Rossi, Ph.D.
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Curriculum Vitae

Present Positions

- *Tenure Track Assistant Professor* in Electronics at Energy Efficient Embedded Systems Lab, Department of Electrical, Electronic and Information Engineering "Guglielmo Marconi" (DEI) of University of Bologna (since November, 2018).
- *Member* of Center for Industrial Research on Information and Communication Technologies (CIRI ICT) of the University of Bologna (since 2016).
- Member of ARCES - Advanced Research Center on Electronic Systems "Ercole De Castro" of the University of Bologna (since 2020).
- Member of Alma AI - Alma Mater Research Institute for Human-Centered Artificial Intelligence of the University of Bologna (since 2021).s

Fellowships and Visiting Positions

- *Visiting Assistant Professor* at the Integrated System Laboratory (IIS) of Eidgenössische Technische Hochschule Zürich (ETHZ) (Sep. - Nov. 2017, Sep. - Nov. 2018).

Experience

- *Post Doc Researcher* at Energy Efficient Embedded Systems Lab, Department of Electrical, Electronic and Information Engineering "Guglielmo Marconi" (DEI) of University of Bologna (2013 - 2015).
- *Ph. D. student* at Advanced Research Center on Electronics Systems, Univ. Bologna (2009 - 2012).
- *Junior Member of R&D Staff*, STMicroelectronics, Agrate Brianza, Italy (2008 - 2012).
- *Research Assistant* at Tampere University of Technology, Tampere, Finland (2005).

Education

- Ph.D. in *Electronics, Telecommunications, and Information Technologies Engineering*, University Of Bologna, 2012.
- M.Sc. in Electronics Engineering**,** University of Bologna/Tampere University of Technology, 2007 (grade: 104/110).
- B.Sc. Electronics Engineering**,** University of Bologna, 2004 (grade: 105/110).

Qualifications

- National Academic Qualification for Associate Professor, Scientific Disciplinary Sector ING-INF 01 (valid from 20/07/2017 to 20/07/2023).
- National Academic Qualification for Associate Professor, Scientific Disciplinary Sector ING-INF 05 (valid from 26/07/2018 to 26/07/2024).

Scientific Profile

Research Activities

My research interests are on computing systems architecture and design of digital integrated systems with special emphasis on low-power architectures, reconfigurable architectures, and related applications. I started my research activities early in my career with an internship at Tampere University of Technology (TUT) during my Master studies, terminated with the master degree at TUT and University of Bologna. The topic of the research was on embedded systems and coarse-grained reconfigurable architectures. In this period, I co-authored two journal papers and three conference papers. At the beginning of my career as a graduate researcher, after one year with ST Microelectronics I started my Ph.D. in the Advanced Research Center on Electronics Systems (ARCES) of University of Bologna where I made several contributions in the field of heterogeneous reconfigurable architectures researching flexible techniques for acceleration of embedded multi-core Systems-On-Chip. I explored two different approaches: the first leveraging heterogeneous reconfigurable fabrics featuring functional units with different granularities, the second leveraging technologies to configure at run-time and design-time the functionalities of the accelerators, exploiting different trade-offs in terms of performance, power and cost. During this period (2009-2012), I designed and taped-out two chips (as main architect and chip designer) and co-authored four journal papers, two book chapters, and four conference papers. In 2013, I joined the Energy Efficient Embedded Systems (EEES) laboratory as a post-doc researcher, where I started my research on near-threshold multi-processing. The ambitious goal of the PULP project I lead (www.pulp-platform.org) is to develop and make research on an open-source, ultra-low-power hardware-software platform for embedded processing in the end-nodes of the IoT, covering all aspects from silicon implementation, programming and applications. I am Chief Architect of the PULP platform, and main responsible for several chips realized in the context of this project. More than 30 companies and universities now use the PULP and related IPs across the world (including Google, Micron, IBM, CEVA, STMicroelectronics, Mentor, Cadence), and I am personally involved in the

development of a product based on PULP with the French start-up GreenWaves Technologies. In these five years, my research has mainly been focused on hardware/software co-design of low-power multi-core embedded platform and related applications. In these fields, I made several contributions on design and programming of low-power multi-core architectures; on embedded applications of low-power architectures, mainly in the fields of embedded vision and processing of biometrical signals; and on emerging technologies for low-power computing such as brain-inspired computing, approximate computing, and transprecision computing. Overall, on the topics listed in this short summary, I co-authored more than 120 papers and three book chapters. I strongly believe in collaborative, multi-disciplinary research. I have an extensive track-record of international cooperation with top-level companies and institutions like: ETHZ, EPFL, CEA, STMicroelectronics, NXP, Tampere University of Technology, Thales, Braunschweig U., Kemnitz U.

A) Teaching

Teaching Activities

During the past years I taught in 4 courses at University of Bologna. The overall number of hours per year taught during last 6 years has been:

- Academic year 2015-2016: 30 hours
- Academic year 2016-2017: 60 hours
- Academic year 2017-2018: 60 hours
- Academic year 2018-2019: 120 hours
- Academic year 2019-2020: 120 hours
- Academic year 2020-2021: 120 hours

More details about the courses can be found below:

- *73801 - LAB OF HARDWARE-SOFTWARE DESIGN M (84419 - LAB OF DIGITAL ELECTRONICS M) - 30 HOURS.* University of Bologna - Academic years 2015-2016, 2016-2017, 2017-2018, 2018-2019, 2019-2020, 2020-2021.
Aim of this course is to enrich the practical experience of the students on advanced digital hardware design tools and methodologies. The students are expected to work on a practical project to deeper their knowledge in digital hardware design, integration of hardware modules into Systems on Chip, and prototyping of digital systems on FPGA devices. The course also covers aspects related to interactions between software and hardware components in Systems on Chip.

- *73731 - ARCHITETTURE E PROGRAMMAZIONE DEI SISTEMI ELETTRONICI T-A - Modulo 2 (29035 - LABORATORIO DI ARCHITETTURE E PROGRAMMAZIONE DEI SISTEMI ELETTRONICI INDUSTRIALI T-A- Modulo 2) – 30 HOURS. Academic years 2016-2017, 2017-2018, 2018-2019, 2019-2020, 2020-2021.*
Aim of this course is to teach the architecture of micro-controller based systems using ARM cortex M cores, and firmware programming for industrial applications. It covers both theoretical and practical aspects related to architecture and programming of ARM Cortex M microcontrollers.

- 73388 - DIGITAL SYSTEMS M - 60 HOURS CFU - 2018-2019
Aim of this course is to provide a vision of digital circuits at transistor and gate level so as to have clear ideas about the main factors determining circuit performance, power consumption, signal integrity digital throughput.

- 93390 - DIGITAL SYSTEMS AND INTRODUCTION TO COMPUTER ARCHITECTURES M - Modulo 1 (84447 - INTRODUCTION TO COMPUTER ARCHITECTURES M) - 60 HOURS - 2019-2020, 2020-2021
Aim of this course is to provide a vision of digital circuits at transistor and gate level so as to have clear ideas about the main factors determining circuit performance, power consumption, signal integrity digital throughput. Overview of digital circuits at logic and register transfer level. Overview of microprocessor and memory architectures. Basics of testing, performance and power consumption at system level.

For more information, visit my personal page: https://www.unibo.it/sitoweb/davide.rossi/didattica

Summer Schools for Ph.D. Students

- D. Rossi, *Parallel Ultra Low-Power Processing (PULP) Systems*, Nips Summer school, 19/07/2018, Perugia, Italy.

- D. Rossi, *PULP: A Multi-Core Platform for Micropower In-Sensor Analytics*, Nips Summer school, 03/09/2019, Perugia, Italy.

- D. Rossi, Digital computing platforms for near-sensor processing at the extreme edge of the IoT, 05/07/2021, SIE Summer School, Trieste, Italy.

Support Activities

During last years I have been tutor of one bachelor course for 2 years, advisor of 11 bachelor theses, 8 master theses, co-advisor of 1 master thesis, advisor of 2 Ph.D. students, co-advisor of 3 Ph.D. students, responsible for 5 research grants. Moreover I co-supervised other 8 Ph.D. students, even if not formally, as demonstrated by a number of joint publications reported in section B) Research. More information about teaching support activities can be found below.

Tutor Activities

- *28727 - PROGETTO DI SISTEMI ELETTRONICI T-A (Tutor)*. University of Bologna, Academic Years 2010-2011, 2011-2012.
Aim of this course is to teach the basics of digital hardware design, RTL hardware description languages and implementation of digital circuits on FPGA devices.

Advisor of Bachelor Theses

- Lorenzo Selvatici, Thesis Title: “CNN2FPGA - A Convolutional Neural Network Compiler for FPGA”, 23/07/2018.

- Annachiara Biguzzi, Thesis Title: “Towards Hardware Implementation of Real-Time Spike Sorting Algorithms”, 05/10/2018.

- Armando Armerì, Thesis Title: “Implementazione ed ottimizzazione di una rete convoluzionale MobileNet quantizzata su architettura ARM Cortex-M7”, 20/12/2018.

- Rea Dizdari, Thesis Title: “Modellazione del background basata su Gaussian mixture model su sistema a microcontrollore”, 20/12/2018.

- Michele Gazzarri, Thesis Title: “Progettazione e sviluppo di un sistema di acquisizione dati per banchi prova sospensioni”, 15/03/2019.

- Luca Serfilippi, Thesis Title: “Architettura di sistema del firmware di un nano-drone intelligente e analisi dell’ integrabilità in un system-on-chip ad alta efficienza energetica”, 3/10/2019.

- Nicolas Bruscoli, Thesis Title: “Progettazione e realizzazione di una toolchain Simulink per processori Zynq”, 19/12/2019.

- Giovanni Giannone, Thesis Title: “Ottimizzazione di una libreria per il calcolo della FFT sviluppata su architettura PULP e adattata per la piattaforma ARM”, 11/03/2020.

- Luca Barbieri, Thesis Title: “Analisi comparativa di algoritmi paralleli di decomposizione QR per l'elaborazione di biosegnali su architettura PULP”, 09/10/2020.

- Veronica Gavagna, Thesis Title: “Progetto di un sistema automatico per il monitoraggio della produzione di rifiuti riciclabili basato su tecnologia IoT”, 09/10/2020.

- Paolo Carboni, Thesis Title: “Estensione dell'ISA di un processore RISC per supportare reti neurali quantizzate a precisione mista” 10/03/2021.

Advisor of Master Theses

- Velu Prabhakar Kumaravel, Thesis Title: “Experimental Evaluation of BITalino: a low-cost modular platform for biosignals acquisition”, 16/03/2018.

- Weiwei Liao, Thesis Title: “low power serial chip-to-chip communication link for ultra low power IoT end nodes”, 24/07/2018.

- Hunaina Farid, Thesis Title: “Influence of Partial Dynamic Reconfiguration on Power Consumption of FPGA Based Implementations”, 23/07/2019.

- Giovanni Landi, Thesis Title: “Design of the Park Assist Based on a Rear Corner Radars and Rear-View Camera Sensor Fusion Strategy”, 24/10/2019.

- Gianmarco Ottavi, Thesis Title: “Sviluppo e Ottimizzazione di un Processore Configurabile con Unità di Calcolo a Precisione Variabile”, 19/12/2019.

- Luca Bertaccini, Thesis Title: “Design of a Cluster-Coupled Hardware Accelerator for FFT Computation”, 06/02/2020.

- Nazareno Bruschi, Thesis Title: “Accelerating Mixed-Precision Quantized Neural Networks on Parallel Ultra Low Power - IoT End Nodes”, 11/03/2020.

- Ilario Coppola, Thesis Title: “A Reconfigurable MIMD/SIMD RISC-V Cluster for Energy-Efficient Parallel Computing”, 11/03/2020.

Co-Advisor of Master Theses

- Marco Donato Torsello, Thesis Title: “Utilizzo di metodi di configurazione automatica per un’applicazione di trans-precision computing su piattaforma PULP”, 06/10/2017.

Advisor of Ph.D. Students

- *Jie Chen (University of Bologna, ETIT, 34° Cycle),* Research Topic: Design and Optimization of the Memory Hierarchy of Parallel-Ultra-Low Power Architectures.

- *Nazareno Bruschi (University of Bologna, ETIT, 36° Cycle),* Research Topic: Parallel computing architectures for heterogenous acceleration of AI algorithms

Co-Advisor of Ph.D. Students

- *Enrico Tabanelli (University of Bologna, ETIT, 35° Cycle),* Research Topic: Acceleration of learning algorithms for parallel ultra-low power processing systems.

- *Alessio Burello (University of Bologna, ETIT, 35° Cycle),* Research topic: Edge machine learning algorithms for the IoT.

- *Luca Valente, (University of Bologna, ETIT, 36° Cycle),* Research Topic: Parallel Ultra-Low Power Processing for the IoT-Ultra Low-Power electronic systems.

Responsible of Research Grants (Assegni di Ricerca)

- *Giuseppe Tagliavini, Research Topic: “*Progetto ed ottimizzazione di un sistema runtime parallelo per piattaforme embedded many-core con requisiti real-time”, 01/04/2016, 23 months.

- *Alessandro Capotondi,* Research Topis: “Valutazione di un sistema runtime parallelo per piattaforme embedded many-core con requisiti real-time”, 06/07/2016, 13 months.

- *Gianmarco Ottavi*, “Design of In-memory computing accelerators for heterogeneous many-core architectures”, 26/11/2019, 24 months.

- *Hayate Okhurawa*, Tecniche di gestione del consumo di potenza “variation aware” per Muti-Cores ad alta efficienza energetica, 06/02/2020, 12 months.

- Nazareno Bruschi, “Applicazioni e Modelli di Programmazione per Architetture di Calcolo Scalabili”, 07/02/2020, 12 months.

Other supervision activities with Ph.D. Students

- *Francesco Conti (University of Bologna).* Hardware blocks for acceleration of convolutional neural networks in programmable deeply embedded system-on-chip.

- *Erfan Azarkhish (University of Bologna).* Exploration of hardware architectures and systems for near-memory computing, exploiting capabilities delivered by new generation 3D stacked memories such as Hybrid Memory Cube.

- *Manuele Rusci (University of Bologna, FBK).* Deeply embedded systems for smart vision coupling analog imagers with energy efficient digital processing platforms.

- *Renzo Andri (ETH Zurich). B*inary convolutional accelerators to enable execution of convolutional neural networks in 10mW power envelope.

- *Satyajit Das (Université de Bretagne-Sud, University of Bologna).* Coarse-grained reconfigurable architectures for acceleration of both data- and control-intensive tasks in the field of IoT applications.

- *Fabio Montagna (University of Bologna).* Design and optimization of bio-signals processing applications on parallel embedded computing platforms.

- *Angelo Garofalo (University of Bologna). Hardware-Software design of Ultra-Low power Multiprocessor Systems on Chip.*

- *Pasquale Davide Schiavone (ETH Zurich). Research Topic: Design of Microprocessors for IoT end-nodes*

B) Research

Research Activities

Impact of Publications

In the last years, I have published (international, peer-reviewed) **48 journal papers 71 conference papers,** and **4 book chapters**. My **h-index is 28, i10-index is 64** (from Google Scholar, July 4th, 2021). The total number of citations is **2654** and the number of citations per year is significantly growing since 2013: **20** in **2013, 34** in **2014, 51** in **2015, 145** in **2016, 310** in **2017, 417** in **2018, 507** in **2019, 702** in **2020, 364** in **2021** (from Google Scholar, on July 4th, 2021).

Scopus Page: https://www.scopus.com/authid/detail.uri?origin=resultslist&authorId=7103169675&zone=
Google Scholar Page: https://scholar.google.it/citations?user=FOkQ6qMAAAAJ&hl=it

Participation to International Conferences as Speaker

- Rossi, F.Campi, A.Deledda, S.Spolzino, S.Pucillo, *A Heterogeneous Digital Signal Processor Implementation for Dynamically Reconfigurable Computing*, Custom Integrated Circuit Conference (CICC), 2009.

- D. Bortolotti, D. Rossi, A. Bartolini, L. Benini, *A Variation Tolerant Architecture for Ultra Low Power Multi-processor Cluster*, International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), 2013.

- D. Rossi, A. Pullini, I. Loi, F. Conti, G. Tagliavini and A. Marongiu, *Energy efficient parallel computing on the PULP platform with support for OpenMP*, 2014 IEEE 28-th Convention of Electrical and Electronics Engineers in Israel, Eilat, Israel, 2014.

- D. Rossi, F. Conti, A. Marongiu, A. Pullini, I. Loi, M. Gautschi, G. Tavaglini, A. Capotondi, P. Flatresse, L. Benini, *PULP: A Parallel Ultra-Low-Power Platform for Next Generation IoT Applications*, Hot Chips: A Symposium on High Performance Chips, 2015.

- D. Rossi, A. Pullini, M. Gautschi, I. Loi; F. K. Gurkaynak, P. Flatresse, L. Benini, *A −1.8V to 0.9V body bias, 60 GOPS/W 4-core cluster in low-power 28nm UTBB FD-SOI technology*, in SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 2015 IEEE , vol., no., pp.1-3, 5-8 Oct. 2015.

- R. Andri, L. Cavigelli, D. Rossi, L. Benini, *YodaNN: An Ultra-Low Power Convolutional Neural Network Accelerator Based on Binary Weights*, ISVLSI 2016.

- D. Rossi et al., "4.4 A 1.3TOPS/W @ 32GOPS Fully Integrated 10-Core SoC for IoT End-Nodes with 1.7μW Cognitive Wake-Up From MRAM-Based State-Retentive Sleep Mode," 2021 IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, CA, USA, 2021.

Participation to National and International Conferences and Workshops as Invited Speaker and Keynote

- D. Rossi, *A 0.44 to 1.2V Voltage, -1.8V to 0.9V Body Bias, 60 GOPS/W 4-core Cluster in conventional-well 28nm UTBB FD-SOI technology*, LetiWorkshop FDSOICE 2015, 22/06/2015, CEA-LETI, Minatec Campus, Grenoble, France. (Invited Talk).

- D. Rossi, *Sub-pj per Operation Scalable Computing with the PULP platform*, Workshop Commissione Calcolo e Reti Istituto Nazionale di Fisica Nucleare (INFN), 19/05/2016, La Biodola, Isola d'Elba, Italy. (Invited Talk).

- D. Rossi, *Sub-pj per Operation Scalable Computing: the PULP experience*, IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 11/10/2016, San Francisco (CA), USA. (Invited Talk).

- D. Rossi, *Sub-pj per Operation Scalable Computing: the next challenge*, 2016 ICSEE International Conference on the Science of Electrical Engineering, 17/11/2016, Eilat, Israel. (Invited Talk).

- D. Rossi, *Smart Integrated Microsystems for the IoT: The Energy Efficiency Challenge*, WEEE 2017, 12/06/2017, Ystad, Sweden. (Invited Talk).

- D. Rossi, *Neurostream: Scalable and Energy Efficient Deep Learning with Smart Memory Cubes*, 23/06/2017, Fraunhofer ITWM, Kaiserslautern, Germany. (Invited Talk).

- D. Rossi, *Sub-pJ per Operation Scalable Computing with the PULP Platform*", MCC2017, 30/11/2017 Uppsala, Sweden (Invited Keynote).

- P. Stenström, D. Rossi, J. Grönqvist, S. Kaxiras, *Is the Multicore dead?,* Multicore Day 2018, Monday, November 29, 2017, Uppsala, Sweden. (Invited Panel)

- D. Rossi, *Ultra-Low-Power Digital Architectures for the Internet of Things*, 14/03/2018, ISQED, Santa Clara, CA, USA (Invited Tutorial).

- *D. Rossi, Quentin: A Near-Threshold SoC for Energy-Efficient IoT End-Nodes in 22nm FDX Technology*, DATE 2018, 22/03/2018, Dresden, Germany. (Invited Talk)

- D. Rossi, *Quentin: An Ultra-Low-Power PULPissimo SoC in 22nm FDX*, IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference, 2018, 15/10/2018 San Francisco, USA. (Invited Talk).

- D. Rossi, *PULP: A Transprecision Multi-Core Platform for Micropower In-Sensor Analytics*, The 16th International System-on-Chip (SoC) Conference, Exhibit, and Workshops, 17/10/2018, Irvine, California. (Invited Talk).

- D. Rossi, *Parallel Ultra-Low-Power Systems*, Bosch, 14/11/2018, Nurmberg, Germany. (Invited Talk).

- D. Rossi, *Mr.Wolf: A RISC-V Parallel Ultra Low Power SoC for IoT Edge Processing*, Multicore Day 2018, Monday, November 26, 2018, Uppsala, Sweden. (Invited Talk).

- D. Rossi, *PULP RISC-V Training*, 24-25/07/2018, Silicon Laboratories (SILABS), Austin, Texas, USA. (Invited Tutorial).

- D. Rossi, *PULP RISC-V Training*, 18-19/09/2018, Silicon Laboratories (SILABS), Rennes, France. (Invited Tutorial).

- D. Rossi, *PULP: An Open-Source RISC-V based Multi-Core Platform for In-Sensor Analytics*, Workshop on Open Source Design Automation (OSDA) at DATE 2019, 29/03/2019, Florence, Italy. (Invited Keynote)

- D. Rossi, *PULP Tutorial*, 13/06/2019, WOSH, ETHZ, Switzerland. (Invited Tutorial).

- D. Rossi, *PULP RISC-V Training*, WISEKEY SA, 18-19/06/2019, Aix-en-Provence, FR. (Invited Tutorial).

- D. Rossi, *PULP: Open Hardware at the Edge of the IoT, WOC, HiPEAC 2020.* (Invited Talk).

- D. Rossi, R. Aitken, E. Alon, B. Khailany, S. Kottapalli, S. Ouyang, D. Patterson, *Is an Open Source Hardware Revolution on the Horizon?*, 18/02/2020, ISSCC 2020, San Francisco, California. (Invited Panel).

- D. Rossi, *PULP Platform Overview*, 03/02/2020 OFA Workshop, Bruxelles. (Invited Talk).

- D. Rossi, *Extending RISC V Platforms for ML at the Extreme Edge of the IoT*, 21/02/2021, ISSCC 2021 FORUM. (Invited Talk).

Organizer and Chair of Special Sessions at National and International Conferences

- L. Benini, D. Rossi, *Parallel Ultra-Low-Power Computing for the IoT: Applications, Platforms, Circuits*, DATE 2017.

- J Nurmi, D. Rossi, C. Malossi, *Approximate and Transprecision Computing Circuits and Systems*, ISCAS 2018.

- D. Rossi, F. Zaruba, T. Benz, L, Bertaccini, *Open Source On-Chip Communication from Edge to Cloud: the PULP experience*, ESWEEK NoCs 2021.

- Session Chair at 2019 26th IEEE International Conference on Electronics, Circuits and Systems Conference in Genova, Italy from 27-29 November 2019, Session: Machine Learning.

National and International Grants (As Principal Investigator)

- *Principal Investigator (March 2016 – July 2018)*: OPEN-NEXT - Strutture software real-time e open-source per piattaforme embedded industriali di prossima generazione (POR-FESR 2014-2020, founded by Regione Emila Romagna, overall project founding € 739.250, UNIBO founding: € 213.000). OPEN NEXT aims at the deployment of multi- and many-core architectures in the fields of industrial automation applications and automotive applications. The key challenge addressed in this project is to enable effective architectural and programming model support to let parallel platforms to meet the strict real-time constraints of industrial applications while delivering significant higher performance and energy efficiency than single-core architectures traditionally employed in applications with real-time constraints. In this project I was main principal investigator and responsible to the activities related to WP2 programming models, leading a team of 2 post doc researchers.

- *Principal Investigator (June 2018 – May 2019)*: EverMORE - Energy-efficient Variation awarE MulticORE (Financial Support to Third Parties from TETRAMAX - TEchnology TRAnsfer via Multinational Application eXperiments, Grant Agreement 761349, overall project founding: € 42.000, UNIBO founding: € 37.000). EVErMORE TTX experiment aims at developing the next generation GAP-8 IoT processor from GreenWaves Technologies (https://greenwaves-technologies.com/). Exploiting the adaptive management architecture for process and temperature compensation developed at University of Bologna, coupled to the low-voltage capabilities of 22nm FD-SOI technology, is expected to significantly improve the energy efficiency of current generation GreenWaves Technology processors, enabling new applications and opening new market opportunities. In this project I was principal investigator and responsible for all the technical and management activities related to the academic partner.

- *Principal Investigator: (Oct 2019 – present)* WiPLASH: Architecting More Than Moore – Wireless Plasticity for Heterogeneous Massive Computer Architectures (GA 863337, overall project founding: € 3 M, UNIBO founding: € 328750). The main design principles in computer architecture have shifted from a monolithic scaling-driven approach towards an emergence of heterogeneous architectures that tightly co-integrate multiple specialized computing and memory units. However, hardware specialization requires interconnection mechanisms that integrate the architecture. However, traditional wired interconnects are unable to provide the efficiency and architectural flexibility required by current and future key ICT applications. WiPLASH project aims to pioneer an on-chip wireless communication plane able to provide architectural plasticity, reconfigurability and adaptation to the application requirements with near-ASIC efficiency but without loss of generality. In this project I'm principal investigator and responsible for WP4 architecture design, leading a team of 3 Ph.D. students and research fellows.

- *Principal Investigator: (Starting in Nov 2021)* The European Pilot: Pilot using Independent Local & Open Technologies (expected overall project founding: € 30 M, expected UNIBO founding: € 842375). The European PILOT (Pilot using Independent Local & Open Technology) will be the first demonstration of two ALL European HPC and High Performance Data Analytics (HPDA) (AI, ML, DL) accelerators, designed, implemented, manufactured, and owned by Europe. The European PILOT combines open source software (SW) and open and proprietary hardware (HW) to deliver the first completely European full stack software, accelerator, and integrated ecosystem based on RISC-V accelerators coupled to any general purpose processor. In this project I will be principal investigator for UNIBO and responsible to all the activities related to the design of machine learning accelerators, leading a team of 6 Ph.D. students and research fellows.

Research Contracts with National and International Private Entities (As Principal Investigator)

- Principal Investigator: (Jan 2021 – present) Elettronica S.p.A. https://www.elt-roma.com/ (€ 25.000). The project aims at the definition of the specifications for a heterogeneous reconfigurable SoC for military applications. In this project I am responsible for the overall contract defining the hardware and software specifications of the system on chip architecture as well as requirements for testing.

- Principal Investigator: (April 2021 – present) (€ 25.000) Technology Innovation Institute https://www.tii.ae/ (€ 750'000). The goal of the project is to develop an open RISC-V-based SoC architecture and software stack for adoption on secure application processors for drone flight computer applications to innovate in processor and platform design co-optimizing security, resilience, power efficiency and real-time performance. In this project I am the principal investigator for UNIBO, responsible for the definition of the specifications of the overall SoC architecture, design and implementation, leading a team of 4 Ph.D. students and research fellow.

Other Activities in National and European Research Projects

- *Leader of power management system design. (Nov 2018 – present) European Processor Initiative (EPI-SGA1) (*overall project founding: 80 M). The European Processor Initiative (EPI) is a project currently implemented under the first stage of

the Framework Partnership Agreement signed by the Consortium with the European Commission (FPA: 800928), whose aim is to design and implement a roadmap for a new family of low-power European processors for extreme scale computing, high-performance Big-Data and a range of emerging applications. In this project I'm leading the design of the power management system, its integration in the final tape-out of the chip, leading a team of 3 Ph.D. students and research fellows.

- *Part of the project technical board (Jan 2017 – Dec 2020).* OPRECOMP (Open transPREcision COMPuting, co-funded by the European Union's H2020-EU.1.2.2. - FET Proactive research and innovation programme, founding: € 4.009.004). OPRECOMP aims at demolishing the ultra-conservative "precise" computing abstraction and replacing it with a more flexible and efficient one, namely transprecision computing. In this project I was senior member of the project technical boards supervising all the activities related to hardware design of a low-power demonstrator for IoT applications.

- *Work Package Leader (Jan. 2008 - Oct. 2009).* WP4 - Platform Integration and monitoring - of project "MORPHEUS" (Multi-purpose dynamically Reconfigurable Platform for intensive Heterogeneous processing, Sixth Framework Programme, overall founding: € 2.463.865). The project aims at developing a global solution based on a modular SoC platform providing the disruptive technology of embedded dynamically reconfigurable computing completed by a software (SW) oriented design flow. In this project I was responsible for the design of the silicon demonstrator of the project in WP3.

- *Task Leader (March 2009 – February 2012).* Task T4.4 - Design of regular architectures and circuits for high manufacturability and yield - of MODERN (MOdeling and DEsign of Reliable, process variation-aware Nanoelectronic devices, circuits and systems, ENIAC-2008-1, overall founding: € 11.816.000). The objective of the MODERN project is to develop new paradigms in integrated circuit design, with the aim of enabling the manufacturing of reliable, low cost, low EMI, high-yield complex products using unreliable and variable devices. In this project I was responsible for the reconfigurable fabrics demonstrators.

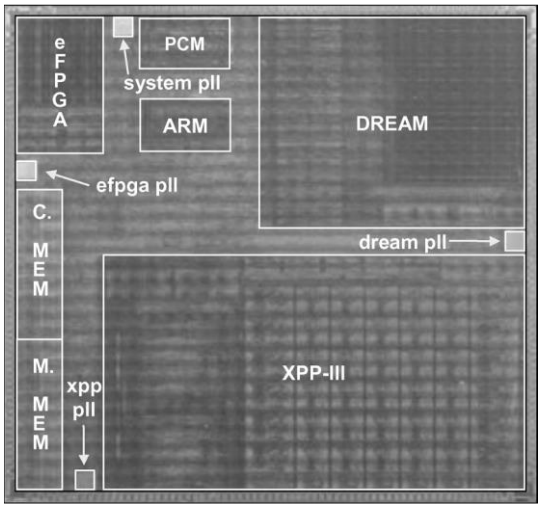
Collaborations with International Research Centers and Companies and Related Achievements

ST Microelectronics (2008 - 2009)

The project introduced one of the first embedded systems on chip architectures exploiting heterogeneous reconfigurable computing where a general-purpose processor is accelerated by multiple flavors of specialized reconfigurable engines for embedded signal processing. This approach is now employed in several fully reconfigurable SoC such as Xilinx Zynq.

Fabricated Prototypes

Morpheus



Process Technology	90 nm CMOS90GP Process, 7-metal layers
Power Supply	1,0V for core, 3,3 for I/0
Area	110 mm^2
Transistor Count	44M Logic 1,1Mbyte SRAM
Pinout	256, 163 I/O
Operating Frequency	ARM, BUS, NoC: 250 MHz XPP : 0 - 160 MHz DREAM : 0 - 200 MHz eFPGA : 0-140 MHz
Power Consumption	Static Power : 235 mW ARM + NoC : 600 mW @ full speed XPP : 1200 mW @ full occupation - full speed DREAM : 420 mW @ full occupation - full speed eFPGA : 112 mW @ full occupation - full speed

Publications

D. Rossi, F. Campi, A. Deledda, S. Spolzino and S. Pucillo, *A heterogeneous digital signal processor implementation for dynamically reconfigurable computing*, 2009 IEEE Custom Integrated Circuits Conference, 2009, pp. 641-644.

D. Rossi, F. Campi, S. Spolzino, S. Pucillo, R. Guerrieri, *A Heterogeneous Digital Signal Processor for Dynamically Reconfigurable Computing*, JSSC IEEE Journal of Solid-State Circuits (JSSC), vol. 45, no. 8, pp. 1615-1626, Aug. 2010.

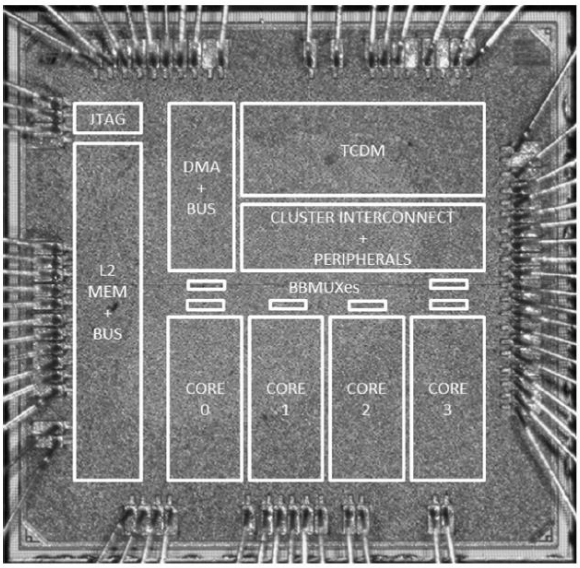
ST Microelectronics, ETH Zurich (2013-2014)

The project explores new programmable multicore architectures that will ease the exploitation of application data-parallelism thanks to an extremely low overhead and efficient multi-core cluster architecture exploiting body-bias technique and low-voltage capabilities of STMicroelectronics 28nm FD-SOI technology. In this project, in collaboration with ETH Zurich, and

which led to 3 joint tape-outs in 28nm FD-SOI and related publications, I was leading a team of 3 Ph.D. students and research fellows.

Fabricated Prototype

PULP



Technology	UTB FDSOI 28nm
Transistors	Conventional well L = 24 nm
Chip area	3 mm^2
VDD range	0.44V - 1.2V
BB range	-1.8V - 0.9V
#SRAM macros	72 x 4 Kbit
Gates	180K
Frequency range	NO BB: 0.74 - 452 MHz FBB: 1.8 - 475 MHz
Power range	NO FBB: 0.1 - 119 mW FBB: 0.11 - 127 mW

Publications

D. Rossi, A. Pullini, M. Gautschi, I. Loi; F. K. Gurkaynak, P. Flatresse, L. Benini, A −1.8V to 0.9V body bias, 60 GOPS/W 4-core cluster in low-power 28nm UTBB FD-SOI technology, in SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 2015 IEEE , vol., no., pp.1-3, 5-8 Oct. 2015.

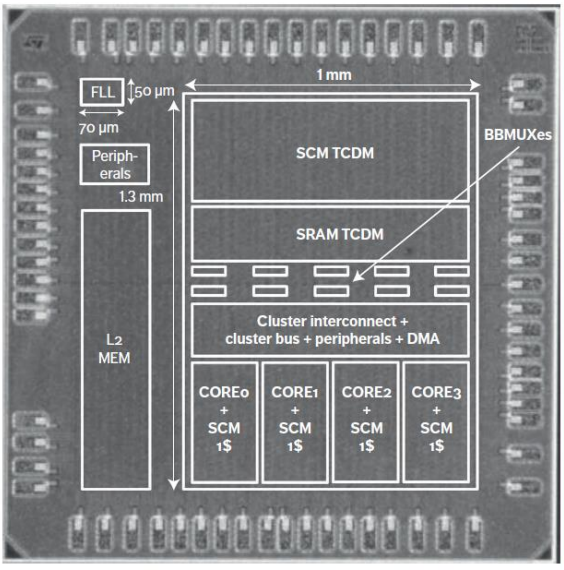
D. Rossi, A. Pullini, I. Loi, M. Gautschi, F. K. Gürkaynak, A. Bartolini, P. Flatresse, L. Benini, A 60 GOPS/W, -1.8V to 0.9V Body Bias ULP Cluster in 28nm UTBB FD-SOI technology", Elsevier Journal of Solid State Electronics, 2016.

ST Microelectronics, ETH Zurich, CEA, EPFL (2014-2016)

Project aimed at the development of a near-threshold parallel architecture exploiting low-power IPs such as low-power processors, memories, power management IPs, and dynamic reconfiguration techniques to break the pj/OP wall in next generation computing architectures for IoT applications. In this project, which lead to a joint tape-out in 28nm FD-SOI and related publications I was leading a team of 5 people from CEA, EPFL, ETHZ and UNIBO.

Fabricated Prototypes

PULP2



Technology	UTBB FD-SOI 28 nm
Transistors	Flip well L = 24 nm
Cluster area	1.3 mm^2
V_{DD} range (SRAMs)	0.32 – 1.15 V (0.45 – 1.15 V)
BB range	0 – 1.75 V
SRAM macros	8 x 32 Kbits (TCDM)
SCM macros	16 x 4 Kbits (TCDM) 4 x 2 x 4 Kbits (1$)
Gates	200K
Frequency range	NO BB: 40.5 – 710 MHz MAX FBB: 63.5 – 825 MHz
Power range	NO FBB: 0.56 – 85 mW MAX FBB: 6.9 – 480 mW

Publications

D. Rossi, A. Pullini, I. Loi, M. Gautschi, F. K. Gurkaynak, A. Teman, J. Constantin, A. Burg, I. M. Panades, E. Beignè, F. Clermidy, F. Abouzeid, P. Flatresse, L. Benini, 193 MOPS/mW @ 162 MOPS, 0.32V to 1.15V Voltage Range Multi-Core Accelerator for Energy-Efficient Parallel and Sequential Digital Processing, Cool Chips, 2016.

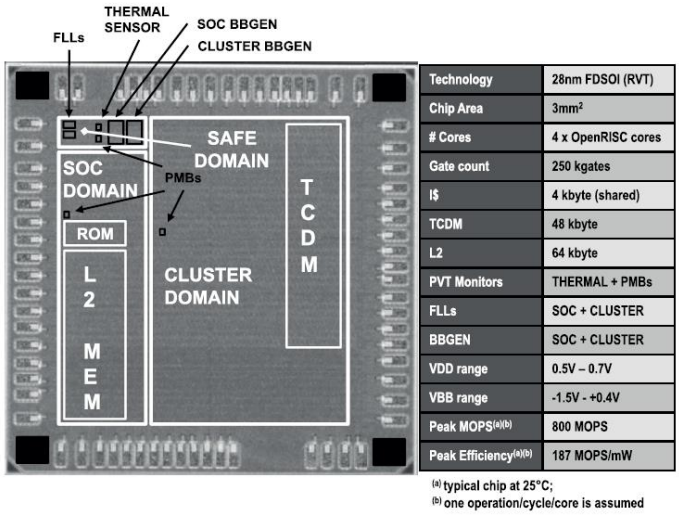
D. Rossi, A. Pullini, I. Loi, M. Gautschi, F. K. Gürkaynak, A. Teman, J. Constantin, A. Burg, I. Miro-Panades, E. Beignè, F. Clermidy, P. Flatresse, L. Benini, Energy-Efficient Near-Threshold Parallel Computing: The PULPv2 Cluster, in IEEE Micro, vol. 37, no. 5, pp. 20-31, September/October 2017.

STMicroelectronics, SOITEC, ETHZ, EPFL (2015 - 2018)

Process and Temperature Compensation with bosy-biasing in 28nm FD-SOI. This project, in collaboration with ETH Zurich, aimed at building a demonstrator of a system with in-the loop process and temperature compensation exploiting the body bias capabilities of 28nm FD-SOI technology. In this project I was supervising the activities of a Ph.D. student in ETH Zurich.

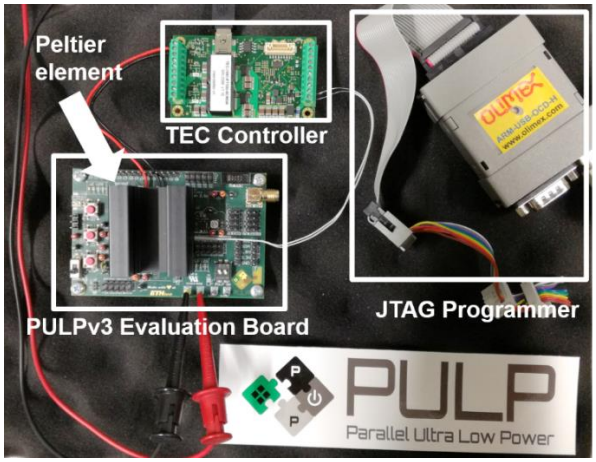
Fabricated Prototypes

PULP3



Technology	28nm FDSOI (RVT)
Chip Area	3mm²
# Cores	4 x OpenRISC cores
Gate count	250 kgates
I$	4 kbyte (shared)
TCDM	48 kbyte
L2	64 kbyte
PVT Monitors	THERMAL + PMBs
FLLs	SOC + CLUSTER
BBGEN	SOC + CLUSTER
VDD range	0.5V – 0.7V
VBB range	-1.5V - +0.4V
Peak MOPS[a][b]	800 MOPS
Peak Efficiency[a][b]	187 MOPS/mW

[a] typical chip at 25°C;
[b] one operation/cycle/core is assumed



Publications

D. Rossi, A. Pullini, C. Muller, I. Loi, F. Conti, A. Burg, P. Flatresse, L. Benini, A Self-Aware Architecture for PVT Compensation and Power Nap in Near Threshold Processors, in IEEE Design & Test, vol. 34, no. 6, pp. 46-53, Dec. 2017.

A. Di Mauro, D. Rossi, A. Pullini, P. Flatresse and L. Benini, Temperature and process-aware performance monitoring and compensation for an ULP multi-core cluster in 28nm UTBB FD-SOI technology, 2017 27th International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS), Thessaloniki, Greece, 2017, pp. 1-8.

A. Di Mauro, D. Rossi, A. Pullini, P. Flatresse and L. Benini, Live Demonstration: Body-Bias Based Performance Monitoring and Compensation for a Near-Threshold Multi-Core Cluster in 28nm FD-SOI Technology, 2018 IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, 2018, pp. 1-1.

NXP (2013-2017)

Project exploring variation-aware multi-core architectures exploiting system monitors (temperature monitors, timing monitors, power monitors) for applying run-time management techniques to achieve the user/application goals in terms of Quality of Service, energy consumption and results reliability/accuracy in next generation low-power microcontrollers. In this project, which led to a joint patent, I was supervising one research fellow.

Publications

A. Gomez, C. Pinto, A. Bartolini, D. Rossi, H. Fatemi, J. Pineda de Gyvez, and L. Benini, Reducing Energy Consumption in Microcontroller-based Platforms with Low Design Margin Co-Processors, Design, Automation & Test in Europe Conference & Exhibition (DATE), 2015.

A. Gomez, A. Bartolini, D. Rossi, B. Can Kara, H. Fatemi, J. P. de Gyvez, L. Benini, Increasing the Energy Efficiency of Microcontroller Platforms with Low-Design Margin Co-Processors, Microprocessors and Microsystems, Available online 24 May 2017, ISSN 0141-9331, https://doi.org/10.1016/j.micpro.2017.05.012.

Patents

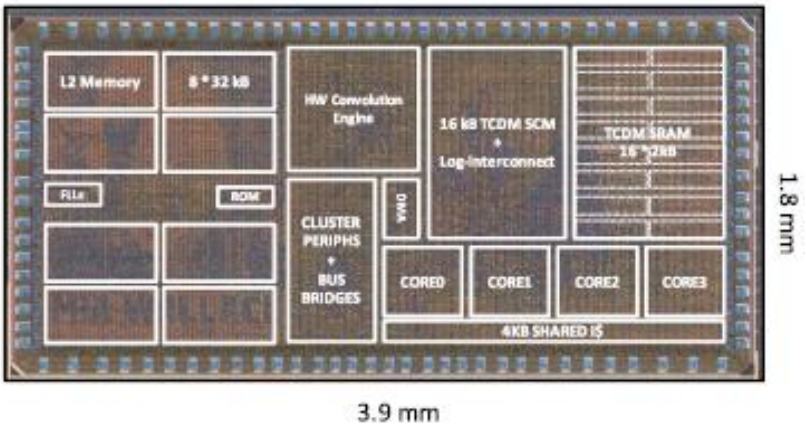
Event-Based Power Manager, published on 2019-05-16 to USPTO (United States Patent and Trademark Office: https://uspto.report/patent/app/20190146566).

ETHZ (2016)

Fabricated Prototypes

Developing the first Parallel Ultra Low Power (PULP) SoC featuring a deep neural network accelerator. In this project I was co-supervising a team of 3 Ph.D. student in ETH Zurich and I was responsible for the design of the architecture specifications and the physical implementation.

Mia Wallace



Publications

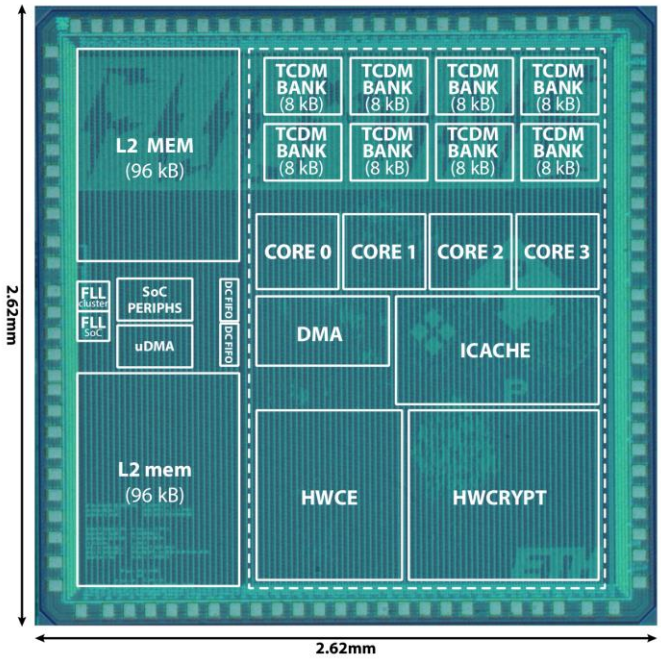
A. Pullini, F. Conti, D. Rossi, I. Loi, M. Gautschi and L. Benini, A Heterogeneous Multicore System on Chip for Energy Efficient Brain Inspired Computing, in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 8, pp. 1094-1098, Aug. 2018, doi: 10.1109/TCSII.2017.2652982.

ETHZ, TU Gratz (2016 - 2017)

This project developed a Parallel Ultra Low Power SCoC combining workload of analytics and encryption in a tight power envelope, called Fulmine. The SoC based on a tightly-coupled multi-core cluster augmented with specialized blocks for compute-intensive data processing and encryption functions, supports software programmability for regular computing tasks.

Fabricated Prototypes

Fulmine



Publications

F. Conti, R. Schilling, P. D. Schiavone, A. Pullini, D. Rossi, F. K. Gürkaynak, M. Muehlberghuber, M. Gautschi, I. Loi, G. Haugou, S. Mangard, L. Benini, "An IoT Endpoint System-on-Chip for Secure and Energy-Efficient Near-Sensor Analytics", in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 64, no. 9, pp. 2481-2494, Sept. 2017.

QuickLogic, ETHZ (2017 – 2019).

Heterogeneous SoC with embedded FPGA. This project, in collaboration also with ETH Zurich, aimed at developing a demonstrator of a heterogeneous SoC integrating an IoT processor with an embedded FPGA from the industrial party. In this project, which led to a tape-out in 22nm FD-SOI technology and a joint TVLSI publication I was supervising a Ph.D. student in ETH Zurich responsible for the design of the architecture and the physical implementation.

Fabricated Prototypes

Arnold

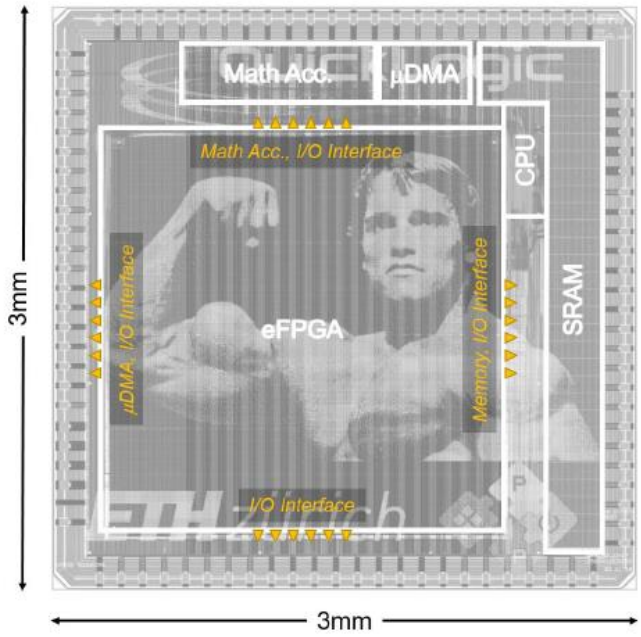


TABLE III
AREA DISTRIBUTION OF THE MAIN COMPONENTS OF ARNOLD

Module	Area [µm^2]	Percentage
CPU	27′186	0.54%
Main Memory	734′232	14.46%
I/O DMA	21′755	0.43%
eFPGA subsystem	63′946	1.26%
PAD Frame	229′519	4.52%
eFPGA Macro	4′000′000	78.79%

Publications

P. D. Schiavone et al., "Arnold: An eFPGA-Augmented RISC-V SoC for Flexible and Low-Power IoT End Nodes," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 29, no. 4, pp. 677-690, April 2021, doi: 10.1109/TVLSI.2021.3058162.

Dolphin Integration, ETHZ (2017 - 2019)

Power-performance scalable processor for IoT. This project, in collaboration with ETH Zurich, aimed at the design of a power-performance scalable processor for IoT applications demonstrating the low-power capabilities of the analog IPs provided by the industrial partner at system level. In this project I was leading a team of 3 Ph.D. students and research fellows, and led to a joint ESSCIRC publication in 2018 and JSSC publication in 2019.

Fabricated Prototypes

Mr. Wolf

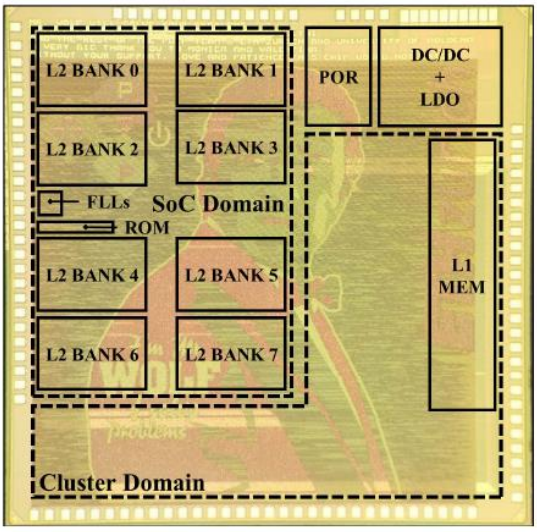


TABLE III
MR. WOLF SOC FEATURES

Technology	CMOS 40nm LP
Chip Area	10mm^2
Memory Transistors	576 kB
Equivalent Gates (NAND2)	1.8 Mgates
Voltage Range	0.8 V – 1.1 V
Frequency Range	32 kHz – 450 MHz
Power Range	72 μW – 153mW

Publications

A. Pullini, D. Rossi, I. Loi, A. Di Mauro, L. Benini, Mr.Wolf: a 1 GFLOP/S Energy-Proportional Parallel Ultra Low Power SoC for IoT Edge Processing, ESSCIRC 2018.

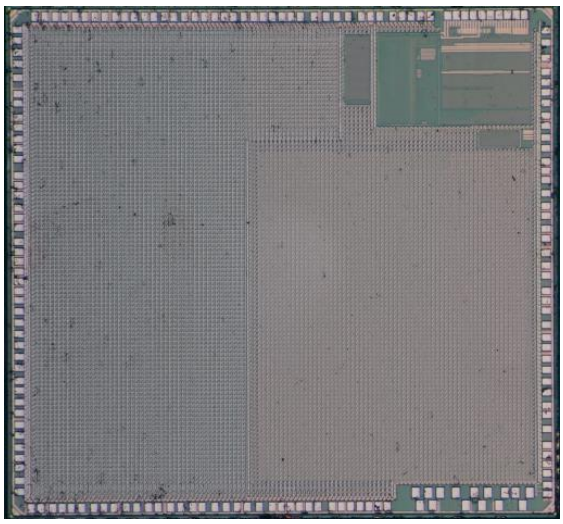
A. Pullini, D. Rossi, I. Loi, G. Tagliavini and L. Benini, "Mr.Wolf: An Energy-Precision Scalable Parallel Ultra Low Power SoC for IoT Edge Processing," in IEEE Journal of Solid-State Circuits, vol. 54, no. 7, pp. 1970-1981, July 2019, doi: 10.1109/JSSC.2019.2912307.

GreenWaves Technologies (2016-2021)

Technology transfer (third mission) activity related to the deployment of the PULP open-source platform to into a commercial system-of-chip (GAP-8) for volume production, and its revision (GAP-9). The main applications targeted by the design are near sensor processing, software defined modem for wireless communication and low power wireless communication for IoT applications (http://greenwaves-technologies.com). In this project I supported technical activities related to the development of the product of the company, and led to a joint ISSCC publication in 2021.

Fabricated Prototypes

GAP8



Technology	CMOS 55nm LP
Die Area	10 mm^2
Embedded Memory	4608 Kbit (4096kbit state-retentive)
Logic Gates	2 Mgates
Power Management	1 DC/DC, 1 LDO, 2 FLLs, embedded power switches
VDD range	0.8V – 1.2V
Frequency Range	32kHz – 250 MHz
Power Range	3.6 µW – 75mW

VEGA

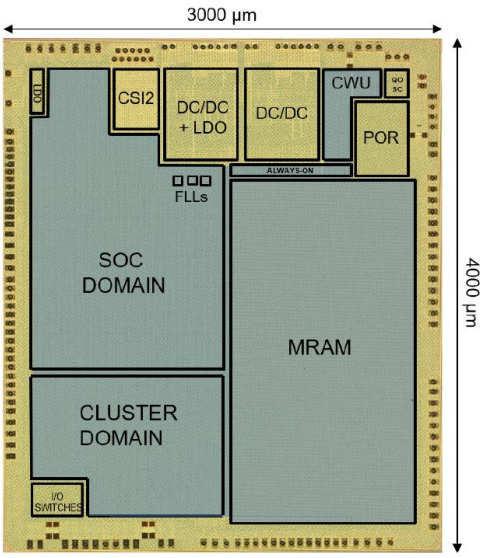


TABLE III
VEGA SOC FEATURES

Technology	CMOS 22nm FD-SOI
Chip Area	$12mm^2$
SRAM Memory	1728 kB
MRAM Memory	4 MB
Equivalent Gates (NAND2)	1.8 Mgates
Voltage Range	0.6 V – 0.8 V
Frequency Range	32 kHz – 450 MHz
Power Range	1.2 μW – 49.4mW

Publications

E. Flamand, D. Rossi, F. Conti, A. Pullini, I. Loi, F. Rotenberg and L. Benini, GAP8: A RISC-V SoC for AI at the Edge of the IoT, 2018 IEEE 29th International Conference on Application-specific Systems, Architectures and Processors (ASAP), 2018.

D. Rossi et al., 4.4 A 1.3TOPS/W @ 32GOPS Fully Integrated 10-Core SoC for IoT End-Nodes with 1.7µW Cognitive Wake-Up From MRAM-Based State-Retentive Sleep Mode, 2021 IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, CA, USA, 2021, pp. 60-62, doi: 10.1109/ISSCC42613.2021.9365939.

D. Rossi et al., Vega: A Ten-Core SoC for IoT Endnodes With DNN Acceleration and Cognitive Wake-Up From MRAM-Based State-Retentive Sleep Mode, in IEEE Journal of Solid-State Circuits, doi: 10.1109/JSSC.2021.3114881.

Dolphin Integration (2019 - present)

AI capable edge processor. This project, in collaboration with ETH Zurich, aims at developing a low-power digital signal processor for embedded video and audio applications featuring capabilities of running embedded machine learning and artificial intelligence workloads, in this project I'm leading a team of 5 Ph.D. Students and research fellows. A tape out in 22nm FD-SOI technology is expected in July 2021.

Facebook (2020 – present)

Low-power processor for augmented reality. This project, in collaboration with ETH Zurich, aims at developing an embedded processor for augmented reality applications, featuring embedded non volatile memory and capable of running both traditional linear algebra algorithms and artificial intelligence workloads with unprecedent performance and energy efficiency. A tape-out in advanced technology nodes has been achieved in December 2021. In this project I' co-leading a team of 3 Ph.D. students.

Patents

- *Event-Based Power Manager*, published on 2019-05-16 to USPTO (United States Patent and Trademark Office: https://uspto.report/patent/app/20190146566). The patent is in collaboration with NXP. The patent is about power management policies in ultra-low-power architectures performing digital signal processing. In particular it envision the adaptation of functional characteristics of microcontrollers (e.g. voltage supply, operating frequency), on the basis of information collected from performance counters available within the architecture, easing the power management to the end-user making them pro-active, hence more effective.

Awards

- *2019 IEEE TCAD Donald O. Pederson Best Paper Award*: R. Andri, L. Cavigelli, D. Rossi and L. Benini, "YodaNN: An Architecture for Ultralow Power Binary-Weight CNN Acceleration," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 37, no. 1, pp. 48-60, Jan. 2018.

- *2019 ISLPED Design Contest 2nd prize award*: Daniele Palossi, Francesco Conti, Davide Rossi, Luca Benini, "PULP-DroNet: Open Source and Open Hardware Artificial Intelligence for Fully Autonomous Navigation on Nano-UAVs", ISLPED 2019 : ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED 2019).

- I4MS-SAE label received by EVErMORE poject, recognising its excellent implementation, high potential for further deployment and innovative aspect.

- 2020 IEEE Transactions on Circuits and Systems Darlington Best Paper Award: F. Conti, R. Schilling, P. D. Schiavone, A. Pullini, D. Rossi, F. K. Gürkaynak, M. Muehlberghuber, M. Gautschi, I. Loi, G. Haugou, S. Mangard, L. Benini, “An IoT Endpoint System-on-Chip for Secure and Energy-Efficient Near-Sensor Analytics”, in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 64, no. 9, pp. 2481-2494, Sept. 2017.

- 2020 IEEE Transactions on Very Large Scale Integration Systems Prize Paper Award: M. Gautschi, P. D. Schiavone, A. Traber, I. Loi, A. Pullini, D. Rossi, E. Flamand, F. K. Gurkaynak, L. Benini, "Near-Threshold RISC-V Core With DSP Extensions for Scalable IoT Endpoint Devices," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 10, pp. 2700-2713, Oct. 2017.

Professional Services

- Member of the editorial board of Elsevier Microelectronics Journal.
- Member of the technical program committee in a number of international conferences and symposia (DATE, DSD, ISCAS, VLSI-SOC, MicDAT, MWCAS).
- Publicity chair at ISLPED 2019.
- Reviewer for a number of international journals (IEE TCAS-I, IEEE TCAS-II, IEEE TCAD, IEEE TCSVT, IEEE TECS, IEEE TETC, JLPEA, Microprocessors and Microsystems, TACO).
- Organizer of the main international conference on Open-Source hardware in 2016: ORCONF2016, Oct 7-9 2016, Bologna (orconf.org).
- Member of FOSSI foundation “The Free and Open Source Silicon Foundation” promoting and assisting free and open digital hardware designs and their related ecosystems (fossi-foundation.org).

List of Publications

Journal Papers

1. Claudio Brunelli, Fabio Campi, Claudio Mucci, Davide Rossi, Tapani Ahonen, Juha Kylliäinen, Fabio Garzia, Jari Nurmi, Design space exploration of an open-source, IP-reusable, scalable floating-point engine for embedded applications, Journal of Systems Architecture, Volume 54, Issue 12, 2008, Pages 1143-1154, ISSN 1383-7621, https://doi.org/10.1016/j.sysarc.2008.05.005.

2. D. Rossi, F. Campi, S. Spolzino, S. Pucillo and R. Guerrieri, "A Heterogeneous Digital Signal Processor for Dynamically Reconfigurable Computing," in IEEE Journal of Solid-State Circuits, vol. 45, no. 8, pp. 1615-1626, Aug. 2010, doi: 10.1109/JSSC.2010.2048149.

3. Claudio Brunelli, Fabio Garzia, Davide Rossi, and Jari Nurmi. 2010. A coarse-grain reconfigurable architecture for multimedia applications supporting subword and floating-point calculations. J. Syst. Archit. 56, 1 (January, 2010), 38–47. DOI:https://doi.org/10.1016/j.sysarc.2009.11.003.

4. Grasset, P. Millet, P. Bonnot, S. Yehia, W. Putzke-Roeming, F. Campi, A. Rosti, M. Huebner, N. S. Voros, D. Rossi, "The MORPHEUS Heterogeneous Dynamically Reconfigurable Platform", Int J Parallel Prog 39, 328–356 (2011). https://doi.org/10.1007/s10766-010-0160-3.

5. D. Rossi, C. Mucci, F. Campi, S. Spolzino, L. Vanzolini, H. Sahlbach, S. Whitty, R. Ernst, W. Putzke-Röming, and R. Guerrieri, "Application Space Exploration of a Heterogeneous Run-Time Configurable Digital Signal Processor," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 21, no. 2, pp. 193-205, Feb. 2013, doi: 10.1109/TVLSI.2012.2185963.

6. D. Rossi, C. Mucci, M. Pizzotti, L. Perugini, R. Canegallo and R. Guerrieri, "Multicore Signal Processing Platform With Heterogeneous Configurable Hardware Accelerators," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 9, pp. 1990-2003, Sept. 2014, doi: 10.1109/TVLSI.2013.2280295.

7. E. Azarkhish, D. Rossi, I. Loi and L. Benini, "A Modular Shared L2 Memory Design for 3-D Integration," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, no. 8, pp. 1485-1498, Aug. 2015, doi: 10.1109/TVLSI.2014.2340013.

8. Conti, F., Rossi, D., Pullini, A. et al. PULP: A Ultra-Low Power Parallel Accelerator for Energy-Efficient and Flexible Embedded Vision. J Sign Process Syst 84, 339–354 (2016). https://doi.org/10.1007/s11265-015-1070-9.

9. Davide Rossi, Antonio Pullini, Igor Loi, Michael Gautschi, Frank K. Grkaynak, Andrea Bartolini, Philippe Flatresse, Luca Benini, ”A 60 GOPS/W, -1.8 V to 0.9 V body bias ULP cluster in 28 nm UTBB FD-SOI technology”, Solid-State Electronics, Volume 117, March 2016, Pages 170-184, ISSN 0038-1101, http://dx.doi.org/10.1016/j.sse.2015.11.015.

10. Adam Teman, Davide Rossi, Pascal Meinerzhagen, Luca Benini, and Andreas Burg. 2016. Power, Area, and Performance Optimization of Standard Cell Memory Arrays Through Controlled Placement. ACM Trans. Des. Autom. Electron. Syst. 21, 4, Article 59 (September 2016), 25 pages. DOI:https://doi.org/10.1145/2890498.

11. M. Rusci, D. Rossi, M. Lecca, M. Gottardi, E. Farella and L. Benini, "An Event-Driven Ultra-Low-Power Smart Visual Sensor," in IEEE Sensors Journal, vol. 16, no. 13, pp. 5344-5353, July1, 2016, doi: 10.1109/JSEN.2016.2556421.

12. E. Azarkhish, C. Pfister, D. Rossi, I. Loi and L. Benini, "Logic-Base Interconnect Design for Near Memory Computing in the Smart Memory Cube," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 1, pp. 210-223, Jan. 2017, doi: 10.1109/TVLSI.2016.2570283.

13. M. Gautschi et al., "Near-Threshold RISC-V Core With DSP Extensions for Scalable IoT Endpoint Devices," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 10, pp. 2700-2713, Oct. 2017, doi: 10.1109/TVLSI.2017.2654506.

14. Pullini, F. Conti, D. Rossi, I. Loi, M. Gautschi and L. Benini, "A Heterogeneous Multicore System on Chip for Energy Efficient Brain Inspired Computing," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 8, pp. 1094-1098, Aug. 2018, doi: 10.1109/TCSII.2017.2652982.

15. F. Conti, R. Schilling, P. D. Schiavone, A. Pullini, D. Rossi, F. K. Gürkaynak, M. Muehlberghuber, M. Gautschi, I. Loi, G. Haugou, S. Mangard, L. Benini, "An IoT Endpoint System-on-Chip for Secure and Energy-Efficient Near-Sensor Analytics," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 64, no. 9, pp. 2481-2494, Sept. 2017, doi: 10.1109/TCSI.2017.2698019.

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Book Chapters

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C) Institutional Activities

Boards

- Member of Engineering and Information Technology for Structural and Environmental Monitoring and Risk Management (EIT4SEMM), University of Bologna, academic board since 2020.

Committees

- Participation to Master Degree Evaluation Committee in Electronics Engineering 23/07/2019
- Participation to Bachelor Degree Evaluation Committee in Automation Engineering 03/10/2019
- Participation to Master Degree Evaluation Committee in Advanced Automotive Engineering 24/10/2019

- Participation to Master Degree Evaluation Committee in Electronics Engineering	19/12/2019
- Participation to Master Degree Evaluation Committee in Electronics Engineering	06/02/2020
- Participation to Master Degree Evaluation Committee in Electronics Engineering	11/03/2020
- Participation to Bachelor Degree Evaluation Committee in Automation Engineering	09/10/2020
- Participation to TOLC (TEST ON LINE CISIA) Evaluation Committee	08/02/2021
- Participation to two Research Fellows Evaluation Committees	13/06/2019
- Participation to one Research Fellow Evaluation Committee	21/06/2019
- Participation to two Research Fellows Evaluation Committees	26/07/2019
- Participation to two Research Fellows Evaluation Committees	19/09/2019
- Participation to one Research Fellow Evaluation Committee	26/09/2019
- Participation to one Research Fellow Evaluation Committee	13/01/2020
- Participation to one Research Fellow Evaluation Committee	17/01/2020
- Participation to two Research Fellows Evaluation Committees	24/01/2020
- Participation to three Research Fellows Evaluation Committees	28/02/2020
- Participation to one Research Fellow Evaluation Committee	20/03/2020
- Participation to two Research Fellows Evaluation Committees	17/04/2020
- Participation to one Research Fellow Evaluation Committee	25/06/2020
- Participation to two Research Fellows Evaluation Committees	12/03/2021
- Participation to two Research Fellows Evaluation Committees	26/03/2021
- Participation to two Research Fellows Evaluation Committees	14/05/2021
- Participation to two Research Fellows Evaluation Committees	09/06/2021