Curriculum Vitae of Prof. Cecilia Metra

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Education

- October 1995 – ***Ph.D.*** in Electronic Engineering and Computer Science, University of Bologna (Italy)
- December 1990 - ***Laurea in Electronic Engineering (summa cum laude)***, University of Bologna (Italy)

Record of Employment

- (December 27th, 2015) – ***Confirmed Full Professor in Electronics*** at the University of Bologna
- (December 27th, 2012) – ***Full Professor in Electronics*** at the University of Bologna
- (October 2010) –Qualification as ***Full Professor in Electronics***
- (March 2005) – ***Associate Professor in Electronics*** at the Department of Electronics, Informatics and Systems (DEIS) of the University of Bologna, Italy
- (2020-present) – Affiliation with the ***Alma Mater Research Institute for Human-Centered Artificial Intelligence (Alma AI)*** of the Univ. of Bologna
- (2005-present) – Affiliation with the ***Advanced Research Centre on Electronic Systems for Information and Communication Technologies E. De Castro (ARCES)*** of the Univ. of Bologna
- (2003) - Qualification as ***Associate Professor in Electronics***
- (October 2000- February 2005) – ***Assistant Professor in Electronics*** at the Department of Electronics, Informatics and Systems (DEIS) of the University of Bologna, Italy
    - (August-December 2002) **- Visiting Faculty Consultant** for ***Intel Corporation (Santa Clara, CA)***
- (June 2000) - Qualification as ***Assistant Professor in Electronics***

- (September 1998 – September 2001) - **Visiting Professor** for the Department of Electrical Engineering of the ***University of Washington (Seattle, USA)***

Specialization and Research Interests

Test and design for testability of electronic circuits/systems, reliable, safe, secure and fault-resilient electronic circuits/systems, circuits/systems for Artificial Intelligence (AI), fault tolerance techniques, error-correcting codes, secure communication protocols, photovoltaic and energy harvesting systems, emerging technologies

Activities in Professional Societies

- (2025-2026) – **IEEE Director, Division VIII**
- (2024) –**IEEE Director-Elect, Division VIII**
- (2021) – **IEEE Director-Elect, Division V -** Elected with 3331 votes (56%)
- (2022-2023) – **IEEE Director, Division V**
- (2021) – **IEEE Director-Elect, Division V -** Elected with 3331 votes (56%)
- (2020) – **Past-President** of the **IEEE Computer Society**
- (2019) – **President** of the **IEEE Computer Society**
- (2023-2024) – **Co-Chair** of the ***IEEE Metaverse*** Initiative of **IEEE Future Directions**
- (2021-2024) – **Member** of the **IEEE Conferences Committee**
- (2020-2023) – **Member** of the **IEEE European Public Policy Committee**
- (2022) – **Director Coordinator** of the **IEEE Diversity and Inclusion Committee**
- (2022-2023) – **Director Coordinator** of the **IEEE Awards Board**
- (2023) **Director Coordinator** of the **IEEE European Public Policy Committee**
- (2022-2023) – **Member** of the **IEEE Awards Board**
- (2023) – **Member** of the IEEE AdHoc Committee on *Innovative Funding Models*
- (2023) – **Member** of the IEEE AdHoc Committee on *Coordinating IEEE's Response to Multimedia-Based Digital Reality*

- (2022, 2023, 2024) – **Member** of the IEEE Theodore W. Hissey Outstanding Young Professional Award Committee

- (2022) – **Member** of the **IEEE Diversity and Inclusion Committee**

- (2022) – **Member** of the **IEEE Ad Hoc Committee on the Future of Engagement**

- (2021-2022) – **Chair** of the **ICT Working Group** of the ***IEEE European Public Policy Committee***

- (2020-2023) – **Member** of the **IEEE *Smart Village* Governing Board**

- (2021-2022) – **Member** of the **IEEE Young Professionals Committee**

- (2020-2022) – **Member** of the **IEEE Systems Council Advisory Committee**

- (2019-2022) – **Co-Chair** of the ***Reliable, Safe, Secure and Time Deterministic Intelligent Systems*** Project of the **IEEE Digital Reality Initiative**

- (2019-2022) – **Member** of the ***Steering Committee*** of the **IEEE Digital Reality Initiative**

- (2019-2022) –**Co-Founder and Vice-Chair** of the ***Special Technical Community (STC)*** on ***Reliable, Safe, Secure and Time Deterministic Intelligent Systems*** of the **IEEE Computer Society**

- (2018) – **President-Elect** of the **IEEE Computer Society -** Elected in October 2017 with 3587 votes (65%) from IEEE CS Members

- (2017) – **Vice-President** for ***Member and Geographic Activities*** of the **IEEE Computer Society**

- (2016-2017) – **Member of the IEEE Computer Society Board of Governors** – Elected with 4249 votes from IEEE CS Members

- (2015-2017) – **Member of the IEEE Council on Electronic Design Automation (CEDA) Board of Governors**

- (2013-2015) – **Member of the IEEE Computer Society Board of Governors** – Elected with 4315 votes from IEEE CS Members

- (2018-2021) – **Member of the European Design Automation Association (EDAA) Main Board**

- (2014) – **Vice-President** for ***Technical and Conference Activities*** of the **IEEE Computer Society**

- (2024-2022, 2020-2017, 2015-2014) – **Member** of the ***Executive Committee*** of the **IEEE Computer Society**

- (2023-2021, 2020-2018, 2015) **Member** of the ***Finance Committee*** of the **IEEE CS**

- (2015) – **Secretary** of the ***Executive Committee*** of the **IEEE Computer Society**
- (2015) – **Member** of the ***Executive Committee*** of the ***Technical and Conference Activities Board*** of the **IEEE Computer Society**
- (2020) – **Chair** of the IEEE Computer Society **Nominations Committee**
- (2018) **Chair** of the ***Constitution and Bylaws Committee of the IEEE CS***
- (2017) – **Chair** of the IEEE Computer Society **Taylor L- Booth Award Committee**
- (2020) – **Member** of the **IEEE TAB/PSPB Products and Services Committee**
- (2020) – **Member** of the **IEEE Computer Society** ***Task Force on Diversity & Inclusion***
- (2017-2015) – Member of the **IEEE Computer Society Fellows Evaluation Committee**
- (2018, 2016) – Member of the **IEEE CS Nominations Committee**
- (2012-2013) – **1st Vice-Chair** of th***e IEEE Computer Society Test Technology Technical Council (TTTC)***
- (2013-2012) – **Chair** of the ***Test Technology Educational Program*** of the ***IEEE Computer Society Test Technology Technical Council (TTTC)***
- (2013) – **Member** of the ***Ad-Hoc Conferences Committee*** **of the** ***IEEE Computer Society***
- (2020-2019, 2013) – **Member** of the ***Constitution and Bylaws Committee*** **of the** ***IEEE Computer Society***
- (July 2012-2020) –**Member** of th***e IEEE Computer Society Manuscript Operations Committee***
- (April 2011-2012) –**Member** of th***e IEEE Computer Society Press Operations Committee***
- (2008-2013) – **Chair** of th***e IEEE Computer Society Test Technology Technical Council (TTTC) Communications Group***
- (2004-2007) – **Vice Co-Chair** of th***e IEEE Computer Society Test Technology Technical Council (TTTC) Communications Group***
- (2004-2011) – **Publicity Chair** of the ***Test Technology Educational Program*** of the ***IEEE Computer Society Test Technology Technical Council (TTTC)***
- Member of the **1999, 2001, 2005, 2006, 2007 Technical Meeting Review Committee** of the ***IEEE Computer Society Test Technology Technical Council (TTTC)***

Editorials

- (2018, 2020) **Editor in Chief** of the *IEEE CS "Transactions on Emerging Topics in Computing"*
- (2013-2016) **Editor in Chief** of the *IEEE CS "Computing Now"*
- (2015-2021) **Member of the Editorial Board** of the *"IEEE Design & Test"*
- (2015-2021) **Associate Editor** of the Journal *"Design Automation for Embedded Systems",* Springer
- (2014-2019) **Associate Editor** of the *IEEE CS "Transactions on Computers"*
- (2015-present) **Member** of the **Editorial Advisory Board** of the IEEE ***"The Institute"***
- (2007-2012) **Associate Editor in Chief** of the *IEEE CS "Transactions on Computers"*
- (2004-2006) **Member of the Editorial Board** of the *IEEE CS "Transactions on Computers"*
- (2004-present) **Member of the Editorial Board** of the *"Journal of Electronic Testing: Theory and Applications (JETTA)"*
- (2013-2014) **Member of the Editorial Board** of the *"ACM Transactions on Design Automation of Electronic Systems (TODAES)"*
- (2000 – 2009) **Member of the Editorial Board** of the *"Microelectronics Journal", Elsevier Science*
- (2007-present) **Member of the Editorial Board** of the *"International Journal of Highly Reliable Electronic System Design", International Sciences Press*
- **Guest Editor/Co-Editor** of the**:**
    - **Monthly Theme** on *"Data Storage Reliability in the IoT Era"*, of "**Computing Now"**, August 2017
    - **Special Issue** on *"High Dependability Systems"* of the **"IEEE Transactions on Emerging Topics in Computing",** 2017 (together with M. Sonza Reorda, Politecnico di Torino, Italia)
    - **Special Issue** on *"Emerging Trends and Design Paradigms for Memory Systems and Storage"* of the **"IEEE Transactions on Emerging Topics in Computing",** 2017 (together with R. Aitken, ARM, USA)

- **Monthly Theme** on *"When Radiation Hits Electronic Circuits"*, of "**Computing Now"**, July 2016

- **Monthly Theme** on *"Are Our Electronic Circuits Getting Older?"* of "**Computing Now"**, September 2015

- **Special Section** on *"Concurrent On-Line Testing and Error/Fault Resilience of Digital Systems"* of the "**IEEE Transactions on Computers"**, Third Section of 2010 (together with R. Galivanche (Intel Corporation (USA))

- **Monthly Theme** on "*Microprocessor Test and Reliability Challenges"* of "**Computing Now",** December 2013

- **Special Issue** on the *"Innovations in Testing"* of **"The Journal of Electronic Testing: Theory and Applications (JETTA)",** 2012

- **Special Issue** on *"Testing"* of **"The Journal of Electronic Testing: Theory and Applications (JETTA)",** 2011

- **Special Issue** on the *"IEEE European Test Symposium 2009"* of **"The Journal of Electronic Testing: Theory and Applications (JETTA)"**, 2010

- **Special Issue** on the *"IEEE European Test Symposium 2008"* of **"The Journal of Electronic Testing: Theory and Applications (JETTA)",** 2009

- **Special Section** on "*Computer-Aided Design for Emerging Technologies*" of the **"IEEE Design & Test",** July-August 2007 (together with F. Lombardi, Northeastern Univ, Boston (USA))

- **Special Issue** on *"Design and Test of Systems-On-a-Chip (SOC)"* of the **"IEEE Transactions on Computers",** May 2006 (together with JC Lo (University of Rhode Island, Rhode Island (USA) and F. Lombardi, Northeastern University, Boston (USA))

- **Special Issue** on *"On-Line Testing and Fault Tolerance"* of **"The Journal of Electronic Testing: Theory and Applications (JETTA)"**, 2005 (together with R. Leveugle, Imag, Grenoble (France))

- **Special Issue** on *"Testing at MultiGbit/s Rates"* of the "**IEEE Design & Test"**, July-August, 2004 (together with A. Ivanov (British Coloumbia University, Vancouver (CA)) and F. Lombardi, Northeastern University, Boston (USA))

- **Special Issue** on *"On-Line Testing"* of **"The Journal of Electronic Testing: Theory and Applications (JETTA)"**, 2004 (together with M. Sonza Reorda, Politecnico di Torino, Italy)

- **Special Issue** on the *"8th IEEE International On-Line Testing Workshop"* of **"The Journal of Electronic Testing: Theory and Applications (JETTA)",** 2003 (together with M. Sonza Reorda, Politecnico di Torino, Italy)

- **Special Issue** on the *"7th IEEE International On-Line Testing Workshop"* of **"The Journal of Electronic Testing: Theory and Applications (JETTA)"**, Vol. 18, n. 3, June 2002 (together with D. Nikolos (Univ. of Patras, Greece), J. P. Hayes (Univ. of Michigan, USA) and M. Nicolaidis (iRoC Techn., France))

- **Special Issue** on *"Defect-Oriented Diagnosis for Very Deep Submicron Systems"* of the "**IEEE Design & Test"**, January-February, 2001 (together with F. Lombardi, Northeastern University, Boston, USA)

Awards

- ***IEEE Fellow*** *("for contributions to the on-line testing and fault-tolerant design of digital circuits and systems"),* since January 2014
- ***IEEE Honor Society IEEE-HKN member,*** 2017
- ***IEEE Computer Society Golden Core Member,*** 2007
- ***IEEE Spirit of the Computer Society Award,*** 2020
- ***IEEE Computer Society Certificate of Appreciation***, 2020 (December)
- ***IEEE Computer Society Certificate of Appreciation***, 2018
- ***IEEE Computer Society Certificate of Appreciation***, 2016 (December)
- ***IEEE Computer Society Certificate of Appreciation***, 2016 (November)
- ***IEEE Computer Society Certificate of Appreciation***, 2015
- ***IEEE Computer Society Meritorious Service Award***, 2010
- ***IEEE Senior Member***, 2010
- ***IEEE Computer Society Meritorious Service Award***, 2006
- ***IEEE Computer Society Certificate of Appreciation***, 2004
- ***IEEE Computer Society Certificate of Appreciation***, 2000
- ***Best Paper Award*** of the ***24th IEEE Defect and Fault Tolerance Symposium in VLSI Systems 2009*** (Chicago, Illinois, 7-9 Ottobre 2009), 2009, for the paper entitled: "Novel High Speed Robust Latch", M. Omana, D. Rossi, C. Metra

Patents

- **Co-inventor** of *"A Digital, Parallel, Clock Synchronizer"* (provisional US Patent OTT Ref #2505-3193).

- **Co-inventor** (together with Kleihorst Richard, Nieuwland Andre, Van Dijk Victor, ***Philips Research, Eindhoven, The Netherlands***) of "*Data Communication Using Fault Tolerant Error Correcting Codes and Having Reduced Ground Bounce"* (International Publication Number WO 2005/088465 A1, International Publication Date 22 September 2005).

Activities in IEEE Sponsored Conferences

- **General Chair** of *The IEEE International Symposium on Emerging Metaverse*, Seattle Area, October 21, 2024

- **General Co-Chair** of *The IEEE Computers, Software, and Applications Conference - COMPSAC 2021: Intelligent and Resilient Computing for a Collaborative World*, Online, July 12-16, 2021

- **General Co-Chair** of the *2020 IEEE Technical Meeting on Reliable, Safe, Secure, and Time-Deterministic Intelligent Systems*, Online, September 30 – October 1, 2020

- **General Co-Chair** of the *1st IEEE Computer Society Global Chapter Summit*, Bologna (Italy), December 7, 2019

- **General Co-Chair** of the *2019 IEEE Technical Meeting on Reliable, Safe, Secure, and Time-Deterministic Intelligent Systems*, Bologna (Italy), December 6, 2019

- **General Chair** of the *IEEE VLSI Test Symposium (VTS)*, Maui (Hawai), April 23-25, 2012

- **General Chair** of the *IEEE VLSI Test Symposium (VTS)*, Dana Point (California), May 2-5, 2011

- **Vice-General Co-Chair** of the *IEEE VLSI Test Symposium (VTS)*, Santa Cruz (California), April 18-21, 2010

- **Program Chair** of the *IEEE VLSI Test Symposium (VTS)*, Santa Cruz (California), May 3-7, 2009

- **Program Co-Chair** of the *1st IEEE International Workshop on Design and Test of Nano Devices, Circuits and Systems (NDCS)*, Boston (MA), September 29-30, 2008

- **Program Co-Chair** of the *IEEE VLSI Test Symposium (VTS)*, San Diego (California), 2008

- **Vice-Program Chair** of the *14th IEEE International On-Line Testing Symposium (IOLTS)*, July 7-9, 2008, Rhodes (Greece)

- **Vice-General Chair** of the *13th IEEE International On-Line Testing Symposium (IOLTS),* July 9-11, Crete (Greece), 2007

- **General Co-Chair** of the *12th IEEE International On-Line Testing Symposium (IOLTS),* July 10-12, Lake of Como (Italy), 2006

- **General Co-Chair** of *The 20th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFTS),* Monterey (California, USA), October 3-5, 2005

- **Program Co-Chair** of the *11th IEEE International On-Line Testing Symposium (IOLTS),* July 6-8, Cote Azur (France), 2005

- **Program Co-Chair** of the *10th IEEE International On-Line Testing Symposium (IOLTS),* July 12-14, Madeira (Portugal), 2004

- **Program Co-Chair** of the *9th IEEE International On-Line Testing Symposium (IOLTS),* July 7-9, Kos (Greece), 2003

- **Program Co-Chair** of the *8th IEEE International On-Line Testing Workshop,* July 8-10, Isle of Bendor (France), 2002

- **General Co-Chair** of the *7th IEEE International On-Line Testing Workshop*, July 9-11, Giardini Naxos-Taormina (Italy), 2001

- **General Co-Chair** of *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFTS),* November 1-3, 1999, Albuquerque (New Mexico)

- **Program Co-Chair** of *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFTS),* November 2-4, 1998, Austin (Texas)

- **Past Chair** of the *IEEE VLSI Test Symposium (VTS),* Berkeley (California), April 29 – May 2, 2013

- **Vice-Program Chair** of the *6th IEEE International On-Line Testing Workshop*, July 3-5, 2000, Maiorca (Spain)

- **Vice-Program Co-Chair** of the *5th IEEE International On-Line Testing Workshop*, July 5-7, 1999, Rhodes (Greece)

- **Vice-Program Co-Chair** of the *4th IEEE International On-Line Testing Workshop*, July 6-8, 1998, Capri (Italy)

- **Member of the Steering Committee** of the *IEEE International Symposium on On-Line Testing and Robust System Design* (2017-present)

- **Member of the Steering Committee** of the *IEEE World Forum on Internet of Things* (2015-2016)

- **Member of the Steering Committee** of *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems* (2001-present)

- **Member of the Steering Committee** of the *ACM Computing Frontiers Conference* (2003-2012)

  - **Track Chair** for *Test* of the ***Design, Automation and Test in Europe Conference (DATE),* 2016,** Dresden (Germany), March 14-18, 2016

  - **Track Chair** for the *PhD Forum* of the ***Design, Automation and Test in Europe Conference (DATE),* 2018,** Dresden (Germany), 2018

  - **Track Chair** for the *PhD Forum* of the ***Design, Automation and Test in Europe Conference (DATE),* 2017,** Lausanne (Switzerland), 2017

  - **Track Chair** for *Test* of the ***Design, Automation and Test in Europe Conference (DATE),* 2015**, Grenoble (France), March 9-13, 2015

  - **Track Chair** for *Test and Reliability* of the ***Design, Automation and Test in Europe Conference (DATE),* 2014,** Dresden (Germany), March 24-28, 2014

  - **Topic Coordinator** for *"Product Test"* of the:

    - ***IEEE International Test Conference (ITC) 2013,*** Anaheim (California), September 10-12, 2013

    - ***IEEE International Test Conference (ITC) 2012,*** Anaheim (California), November 4-9, 2012

    - ***IEEE International Test Conference (ITC) 2011,*** Anaheim (California), September 18-23, 2011

- **Topic Coordinator** for *"On-Line Test"* of the:

    - ***IEEE International Test Conference (ITC) 2010,*** Austin (Texas), October 31- November 5, 2010

    - ***IEEE International Test Conference* (ITC) 2009,** Austin (Texas), November 3-5, 2009

    - ***IEEE International Test Conference (ITC) 2008,*** Santa Clara (California), October 28-30, 2008

    - ***IEEE International Test Conference (ITC) 2007,*** Santa Clara (California), October 23-25, 2007

- **Topic Coordinator** for *"On-Line Test"*, for *"Fault Models"* and for *"Design For Availability"* of the:

  - ***IEEE International Test Conference (ITC) 2006,*** Santa Clara (California), October 22-27, 2006

  - ***IEEE International Test Conference (ITC) 2005,*** Austin (Texas), 6-10 November, 2005

  - ***IEEE International Test Conference (ITC) 2004,*** Charlotte (NC), 26-28 October, 2004

- **Topic Coordinator** for *"On-Line Test"* and for *"Fault Models"* of the:

  - ***International Test Conference (ITC) 2003,*** Charlotte (NC), 30 September - 2 October, 2003

  - ***International Test Conference (ITC) 2002,*** Baltimore (MD), October 8-10, 2002

  - ***International Test Conference (ITC) 2001***, Baltimore (MD), 30 October - 1 November, 2001

  - ***International Test Conference (ITC) 2000,*** Atlantic City (NJ), 3-5 October, 2000

- **Program Committee Chair** of ***The First International Conference on Advances in System Testing and Validation Lifecycle (VALID) 2009,*** Porto (Portugal), September 20-25, 2009

- **Topic Chair/Co-Chair** for:

  - *"On-line test, fault tolerance, reliability, dependability and functional safety"* of the

    - ***European Test Symposium (ETS),*** Cyprus (Greece), May 22-25, 2017

  - *"On-line Testing and Reliability"* of the

    - ***European Test Symposium (ETS),*** Avignon (France), 27-31 May, 2013

    - ***European Test Symposium (ETS),*** Annecy (France), May 28-June 1, 2012

  - *"On-line Testing and Fault Tolerance"* of the

    - ***Design, Automation and Test in Europe (DATE) Conference,*** Grenoble (France), March 18-22, 2013

- ✓ ***Design, Automation and Test in Europe (DATE) Conference,*** Dresden (Germany), March 12-16, 2012

➢ *"Testing"* of the

- ✓ ***ACM/IEEE Great Lakes Symposium on VLSI (GLS-VLSI),*** Providence (Massachusetts), May, 2010
- ✓ ***ACM/IEEE Great Lakes Symposium on VLSI (GLS-VLSI),*** Boston (Massachusetts), May 10-12, 2009
- ✓ ***ACM/IEEE Great Lakes Symposium on VLSI (GLS-VLSI),*** Orlando (Florida), May 4-6, 2008

➢ *"On-line Testing, Fault Tolerance and Reliability"* of the

- ✓ ***Design, Automation and Test in Europe (DATE) Conference,*** Grenoble (France), March 14-18, 2011
- ✓ ***Design, Automation and Test in Europe (DATE) Conference,*** Nice (France), April 16-20, 2007
- ✓ ***Design, Automation and Test in Europe (DATE) Conference,*** Munich (Germany), March 6-10, 2006
- ✓ ***Design, Automation and Test in Europe (DATE) Conference,*** Munich (Germany), March 7-11, 2005

➢ *"Field-Oriented Test and On-line Testing"* of the ***Design, Automation and Test in Europe (DATE) Conference,*** Paris (France), February 16-20, 2004

➢ *"On-line Testing and Fault Tolerance"* of the

- ✓ ***European Test Symposium (ETS),*** Freiburg (Germany), May 20-24, 2007
- ✓ ***"European Test Symposium (ETS)",*** Southampton (England), May 21-25, 2006

- **European Liaison** of the:

➢ ***8th IEEE International Workshop on Silicon Debug and Diagnosis*** (SDD), Anaheim, California, 8-9 November, 2012

- **Publication Chair** of the:

➢ ***IEEE European Test Symposium (ETS),*** Trondheim (Norway), May 23-27, 2011

- ***IEEE European Test Symposium (ETS),*** Prague (Czech Republic), May 25-28, 2010
- ***European Test Symposium (ETS),*** Seville (Spain), May 24-28, 2009
- ***European Test Symposium (ETS),*** Lake Maggiore (Italy), May 25-29, 2008

- **Publicity Co-Chair** of the *IEEE VLSI Test Symposium,* Palm Springs (CA), May 1-5, 2005
- **Special Sessions Co-Chair** of the**:**
  - ***IEEE VLSI Test Symposium,*** Berkeley (CA)**,** May 6 – 10, 2007
  - ***IEEE VLSI Test Symposium,*** Berkeley (CA), April 30 – May 4, 2006

- **Member of the Technical Program Committee** of the following International Conferences:
  - *IEEE Latin-American Test Symposium (LATS),* Montevideo (Uruguay), September 5-8, 2022
  - *IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT),* Online, October 6-8, 2021
  - *IEEE Latin-American Test Symposium (LATS),* Punta del Este (Uruguay), October 27-29, 2021
  - *IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT),* Frascati (Italy), October 19-21, 2020
  - *23rd IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems* (DDECS'19), Novi Sad (Serbia), April 22-24, 2020
  - *IEEE Latin-American Test Symposium (LATS),* Jatiúca (Brazil), 30th March - 2nd April 2020
  - *22nd IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems* (DDECS'19), Cluj-Napoca (Romania), April 24-26, 2019
  - *The 27th Asian Test Symposium (ATS18),* Hefei (China), October 15-18, 2018
  - *IEEE Latin-American Test Symposium (LATS),* São Paulo (Brazil), March 13 – 15, 2018
  - *21st IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems* (DDECS'18), Budapest (Hungary), April 25-27, 2018
  - *IEEE International Symposium on On-Line Testing and Robust System Design 2018 (IOLTS 2018),* Platja d'Aro, (Spain), July 2-4, 2018
  - *IEEE European Test Symposium (ETS),* Bremen (Germany), May 28-June 1, 2018

- *The 26th Asian Test Symposium (ATS17),* Taipei (Taiwan), November 27-30, 2017
- *IEEE International Symposium on On-Line Testing and Robust System Design 2017 (IOLTS 2017),* Thessaloniki (Greece), July 3-5, 2017
- *IEEE Latin-American Test Symposium (LATS),* Bogota (Colombia), March 13 – 15, 2017
- *IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT),* Cambridge (UK), October 30 – November 1, 2017
- *IEEE European Test Symposium (ETS),* Cyprus (Greece), May 22-25, 2017
- *The 25th Asian Test Symposium (ATS16),* Hiroshima (Japan), November 21-24, 2016
- *IEEE International Symposium on On-Line Testing and Robust System Design 2016 (IOLTS 2016),* Sant Feliu de Guixols (Spain), July 4-6, 2016
- *IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT),* Storrs (Connecticut, USA), September 19-20, 2016
- *IEEE Latin-American Test Symposium (LATS),* Foz do Iguacu (Brasil), 6-8 Aprile, 2016
- *European Test Symposium (ETS),* Amsterdam (The Netherlands), 23-27 May, 2016
- *IEEE 2nd World Forum on Internet of Things*, December 14-16, 2015, Milan (Italy)
- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems,* Amherst (Massachusetts), October 12-14, 2015
- *21st IEEE International On-Line Testing Symposium,* July 6-8, 2015, Halkidiki (Greece)
- *European Test Symposium (ETS),* Cluj-Napoca (Romania), 25-29 May, 2015
- *20th IEEE International On-Line Testing Symposium,* Platja d'Aro (Spain), July 7-9, 2014
- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems,* Amsterdam, (The Netherlands), October 1-3, 2014
- *The 23rd Asian Test Symposium (ATS11),* Hangzhou, Zhejiang (China), November 16-19, 2014
- *European Test Symposium (ETS),* Paderborn (Germany), 26-30 May, 2014
- *The 22nd Asian Test Symposium (ATS11),* Yilan (Taiwan), Nov. 18-21, 2013
- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems,* New York (USA), October 2-4, 2013
- *19th IEEE International On-Line Testing Symposium,* Chania (Greece), July 8-10, 2013

- *The 21st Asian Test Symposium (ATS11),* Niigata (Japan), Nov. 19-22, 2012
- *18th IEEE International On-Line Testing Symposium,* Sitges (Spain), June 27-29, 2012
- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems*, Austin (Texas), October, 2012
- *17th IEEE International On-Line Testing Symposium,* Athens (Greece), July 13-15, 2011
- *The 20th Asian Test Symposium (ATS11),* New Delhi (India), November 21-23, 2011
- *The 21th International Conference on Field Programmable Logic and Applications*, Chania (Greece), September 5 - 7, 2011
- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems*, Vancouver (Canada), October 3-5, 2011
- *1st Workshop on System Validation and Computer Architecture,* San José (California), June 4, 2011
- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Kyoto (Japan), October 6-8, 2010
- *The Second International Conference on Advances in System Testing and Validation Lifecycle (VALID) 2010*, Nice (France), 22-27 August, 2010
- *4th Workshop on Dependable and Secure Nanocomputing*, Chicago (IL, USA), June 28, 2010
- *The 16th IEEE International On-Line Testing Symposium 2010 (IOLTS 2010)*, Corfù (Greece), July 5-7, 2010
- *IEEE European Test Symposium (ETS),* Prague (Czech Republic), May 25-28, 2010
- *The 20th International Conference on Field Programmable Logic and Applications (FPL),* Milan (Italy), August 31 – September 2, 2010
- *IEEE International Workshop on Reliability Aware System Design and Test (RASDAT'10),* Bangalore (India), January 7-8, 2010
- *6th IEEE International Workshop on Silicon Debug and Diagnosis (SDD10),* Dresden (Germany), March 12, 2010
- *Design, Automation and Test in Europe (DATE) Conference*, Dresden (Germany), March 8-12, 2010
- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Chicago (IL, USA), October 7-9, 2009

- *IEEE International Workshop on Memory Technology, Design, and Testing (MTDT),* Hsinchu (Taiwan), 31 August – 2 September, 2009

- *15th Annual IEEE International Mixed-Signals, Sensors, and Systems Test Workshop (IMS3TW),* Scottsdale (Arizona), June 10-12, 2009

- *European Test Symposium (ETS),* Seville (Spain), May 24-28, 2009

- *15th IEEE International On-Line Testing Symposium*, Sesimbra-Lisbon (Portugal), June 24-27, 2009

- *Design, Automation and Test in Europe (DATE) Conference*, Nice (France), April 20-24, 2009

- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Cambridge-Boston (USA), October 1-3, 2008

- *14th Annual IEEE International Mixed-Signals, Sensors, and Systems Test Workshop (IMS3TW),* Vancouver (Canada), June 18-20, 2008

- *5th IEEE International Workshop on Silicon Debug and Diagnosis (SDD07),* San Diego (California), April 30 – May 1, 2008

- *Design, Automation and Test in Europe (DATE) Conference*, Munich (Germany), March 10-14, 2008

- *European Test Symposium (ETS),* Lake Maggiore (Italy), May 25-29, 2008

- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Rome (Italy), September 26-28, 2007

- *"IEEE/ACM International Symposium on Nano Scale Architectures (Nanoarch'07)",* San Josè (California), October 21-22, 2007

- *IEEE VLSI Test Symposium*, Berkeley (California), May 6—10, 2007

- *2nd IEEE International Workshop on Design for Manufacturability and Yield (DFM&Y 2007),* Santa Clara (CA), October 25-26, 2007

- *4th IEEE International Workshop on Silicon Debug and Diagnosis (SDD07),* Freiburg (Germany), May 23 – 24, 2007

- *1st IEEE International Workshop on Design for Manufacturability & Yield (DFM&Y 2006),* Santa Clara (California), October 26 – 27, 2006

- *43rd Design Automation Conference,* San Francisco (California), July 24 – 28, 2006

- *IEEE VLSI Test Symposium*, Berkeley (California), April 30 – May 4, 2006

- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Washington DC (USA), October 4-6, 2006
- *4th IEEE International Workshop on Infrastructure IP (I-IP),* Berkeley, California, USA, May 4-5, 2006
- *3rd IEEE International Workshop on Silicon Debug and Diagnosis (SDD06),* Santa Clara (California), October 27 – 28, 2006
- *IEEE International Workshop on Memory Technology, Design, and Testing (MTDT),* Tapei (Taiwan), August 3 – 5, 2005
- *2nd IEEE International Workshop on Silicon Debug and Diagnosis (SDD05),* Austin (Texas), November 10 – 11, 2005
- *IEEE VLSI Test Symposium*, Palm Springs (California), May 1 – 4, 2005
- *IEEE European Test Symposium*, Talin (Estonia), May 22 – 25, 2005
- *The 19th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Cannes (France), 10 – 13 October, 2004
- *IEEE International Workshop on Memory Technology, Design, and Testing (MTDT),* San Josè (CA), August 9 – 10, 2004
- *IEEE European Test Symposium*, Ajaccio, Corsica (France), May 23 – 26, 2004
- *3rd IEEE International Workshop on Infrastructure IP (I-IP),* Palm Springs, California, USA, May 4-5, 2005
- *2nd IEEE International Workshop on Infrastructure IP (I-IP),* Charlotte, North Carolina, USA, October 28-29, 2004
- *1st IEEE International Workshop on Silicon Debug and Diagnosis (SDD04),* Ajaccio, Corsica (France), May 26 – 27, 2004
- *IEEE VLSI Test Symposium*, Napa (California), April 26 – 29, 2004
- *ACM Computing Frontiers Conference*, Ischia (Italy), April 14-16, 2004
- *IEEE VLSI Test Symposium*, Napa (California), April 27 - May 1, 2003
- *IEEE European Test Workshop*, Maastricht (The Netherlands), May 25 - 28, 2003
- *Design, Automation and Test in Europe (DATE) Conference*, Munich (Germany), March 3-7, 2003

- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Boston (MA), November, 2003
- *1st IEEE International Workshop on Infrastructure IP (I-IP),* Charlotte, North Carolina, USA, October 2-3, 2003
- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Vancouver (British Columbia), November 6-8, 2002
- *Design, Automation and Test in Europe (DATE) Conference*, Paris (France), March 4-8, 2002
- *IEEE International Workshop on Yield Optimization & Test*, Baltimore (MD, USA), November 1-2, 2001
- *Design, Automation and Test in Europe (DATE) Conference*, Munich (Germany), March 13-16, 2001
- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, San Francisco (CA), October 24-26, 2001
- *IEEE International Workshop on Yield Optimization & Test*, Atlantic City (NJ), October5-6, 2000
- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Mt. Fuji (Japan), October 25-27, 2000
- *Design, Automation and Test in Europe (DATE) Conference*, Paris (France), March 27-30, 2000
- *3rd IEEE International On-Line Testing Workshop,* Crete (Greece), July 7-9, 1997
- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Paris (France), October 20-22, 1997
- *2nd IEEE International On-Line Testing Workshop*, Saint-Jean de-Luz, Biarritz (France), July 8-10, 1996
- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Boston, Massachussets (USA), November 6-8, 1996
- *The IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems*, Lafayette (Louisiana), November 13-15, 1995

- **Co-organizer of the following panels:**
  - *"Challenges for the Metaverse Hardware",* of *The 28th IEEE European Test Symposium,* May 22-26, 2023, Venice (Italy)

- *"Industrial Challenges for Reliable, Safe, Secure and Time Deterministic Intelligent Systems"*, of *The 28th IEEE International Symposium on On-Line Testing and Robust Design*, September 12-14, 2022, Torino (Italy)

- *"Technological and Regulatory Challenges for AI in Europe"*, of the *IEEE World Congress on Computational Intelligence - Industry Day*, July 20, 2022, Padova (Italy)

- *"Technological Challenges for a Smarter World"*, of the *1st IEEE Computer Society Global Chapter Summit*, December 7, 2020, Bologna (Italy)

- "*Challenges for Reliable, Safe, Secure and Time Deterministic Intelligent Systems"*, of the *2019 IEEE Technical Meeting on Reliable, Safe, Secure, and Time-Deterministic Intelligent Systems*, December 6, 2020, Bologna (Italy)

- *"Reliability Issues for Very Deep Submicron ICs",* of the *8th IEEE International On-Line Testing Workshop*, July 8-10, 2002, Isle of Bendor (France). The panel has been co-organized also with the international magazine IEEE Design & Test

- *"Fault-Tolerance: needs and perspectives"*, of the *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, November 2-4, 1998, Austin (Texas). The panel has been co-organized also with the international magazine IEEE Design & Test

- *"Yield, Testing and Reliability Issues for Very Deep Submicron Chips",* of the *IEEE International On-Line Testing Workshop*, July 9-11, 2001, Giardini Naxos-Taormina (Italy). The panel has been co-organized also with the international magazine IEEE Design & Test

- **Organizer of the following Special Sessions:**

  - "*Fault Tolerance Techniques for Memory Reliability Improvement"* for the ***IEEE International Workshop on Memory Technology, Design, and Testing (MTDT),*** San Josè (CA), August 9 – 10, 2004

  - "*Robust Design Techniques for Soft Errors"* for the ***IEEE International On-Line Testing Symposium,*** Saint Raphael (France), July 6 – 8, 2005

  - *"Memory Reliability Challenges"* for the ***IEEE International On-Line Testing Symposium,*** Lake of Como (Italy), July 10 – 12, 2006

  - *"Test and Reliability Challenges for Innovative Systems"* for the ***IEEE International On-Line Testing Symposium,*** Saint Raphael (France), July 6 – 8, 2006

- **Session Chair-Moderator** for the following International Conferences:

  - *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Vancouver (Canada), October 3-5, 2011

  - *Design, Automation and Test in Europe (DATE) Conference*, Grenoble (France), March 14-18, 2011

- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Kyoto (Japan), October 6-8, 2010

- *IEEE East-West Design & Test International Symposium*, Moscow (Russia), September 18-21, 2009
- "*International Test Conference*", Santa Clara (California, USA), October 28-30, 2008 (session 12)
- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Rome (Italy), September 26-28, 2007, *IEEE VLSI Test Symposium*, Berkeley (CA), May 6 – 10, 2007

- *Design, Automation and Test in Europe (DATE) Conference*, Nice (France), April 16-20, 2007

- *43rd Design Automation Conference*, San Francisco (California), July 24 – 28, 2006

- *12th IEEE International On-Line Testing Symposium*, July 10-12, Lake of Como (Italy), 2006

- *IEEE VLSI Test Symposium*, Berkeley (California), April 30 – May 4, 2006

- *9th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems* (DDECS'06), Prague (Czech Republic), April 18 – 21, 2006

- *IEEE VLSI Test Symposium*, Palm Springs (California), May 1 – 4, 2005

- *IEEE International Workshop on Memory Technology, Design, and Testing (MTDT)*, San Josè (CA), August 9 – 10, 2004

- *Design, Automation and Test in Europe (DATE) Conference***,** Munich (Germany), March 6-11, 2005

- *The 19th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Cannes (France), 10 – 13 October, 2004

- *2nd IEEE International Workshop on Infrastructure IP (I-IP)*, Charlotte, North Carolina, USA, October 28-29, 2004

- *IEEE VLSI Test Symposium*, Napa (California), April 26 – 29, 2004

- *ACM Computing Frontiers Conference*, Ischia (Italy), April 14-16, 2004

- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Boston (MA), November, 2003

- *1st IEEE International Workshop on Infrastructure IP (I-IP)*, Charlotte, North Carolina, USA, October 2-3, 2003

- *IEEE European Test Workshop*, Maastricht (The Netherlands), May 25 - 28, 2003
- *IEEE International Workshop on Memory Technology, Design and Testing,* Isle of Bendor (France), July 10-12, 2002
- *8th IEEE International Mixed Signal Testing Workshop*, Montreux (Switzerland), June 18-21, 2002
- *IEEE European Test Workshop*, Corfù (Greece), May 26-29, 2002
- *20th IEEE VLSI Test Symposium*, Monterey (California), April 28 - May 1, 2002
- *4th International Conference on Massively Parallel Computing Systems (MPCS),* Ischia (Italy), April 10-12, 2002
- *Design, Automation and Test in Europe (DATE) Conference*, Paris (France), March 13-16, 2001
- *18th IEEE VLSI Test Symposium, Montreal (Canada),* April 30 - May 4, 2000
- *IEEE International Workshop on Yield Optimization & Test,* Atlantic City (NJ), October 5-6, 2000
- *6th IEEE International On-Line Testing Workshop*, Maiorca (Spain), July 3-5, 2000
- *5th IEEE International On-Line Testing Workshop,* Rhodes (Greece), July 5-7, 1999 *16th IEEE VLSI Test Symposium,* Monterey (California), April 26-30, 1998 *3rd IEEE International On-Line Testing Workshop*, Crete (Greece), July 7-9, 1997
- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Paris (France), October 20-22, 1997

Invited Talks/Tutorials/Lessons/Panels

- **Keynote Speaker** at the ***2024 IEEE 8th International Forum on Research and Technologies for Society and Industry,*** September 18-20, 2024**,** Lecco (Italy), with the talk entitled *"AI Hardware Reliability Risks and Impact on System Safety and Security"*
- **Invited Talk** at the ***1st IEEE RAS in Data Centers Summit,*** Santa Clara (California), June 11-12, 2024, with the talk entitled *"Data Centers' Reliability Risks due to Faults Affecting their High Performance Microprocessors' Caches"*
- **Invited Talk** at the ***IEEE Region 8 Meeting,*** Vienna (Austria), March 2, 2024, with the presentation entitled *"IEEE Metaverse Initiative"*
- **Invited Panelist** at the ***AEIT International Annual Conference***, September 25-27, 2024

- **Invited Speaker** at the (on line) ***IEEE Computer Society Webinar*** entitled *"IEEE Metaverse Initiative and IEEE Computer Society's Involvement in Metaverse Related Standards",* August 29, 2024

- **Keynote Speaker** (online) at the ***5th International Conference on Recent Developments in Control Automation and Power Engineering (RDCAPE) 2023,*** October 12-13, 2023**,** Noida (India), with the talk entitled *"AI Hardware Safety and Reliability Risks to Enable the Future Metaverse"*

- **Invited Speaker** at the ***IEEE AIUB Student Branch,*** September 9, 2023, Online**,** with the talk entitled *"Reliability and Safety Risks for the AI Hardware in the Perspective of the Future Metaverse"*

- **Invited Keynote Speaker** at ***IEEE Region 10 webinar series (R10Talk),*** August 5, 2023, Online**,** with the talk entitled *"Reliability and Safety Challenges for the AI Hardware to Enable the Future Metaverse"*

- **Invited Distinguished Lecturer Talk** for the ***IEEE Consumer Technology Society, IEEE Product Safety Engineering Society, IEEE Broadcast Technology Society***, July 31, 2023, Online, with the talk entitled *"Hardware Reliability and Safety Challenges to Enable a Reliable and Safe AI"*

- **Invited Talk** as **IEEE Division V Director,** at the ***IEEE Region 8 Meeting,*** Bucharest (Romania), March 24-26, 2023

- **Invited Keynote (Visionary Talk)** at the ***ACM/IEEE 60th Design Automation Conference - DAC,*** July 9-13, 2023, San Francisco (California), with the talk entitled *"AI Hardware Reliability and Safety Challenges to Enable the Future Metaverse"*

- **Invited Speaker** at *the* ***IEEE Advanced School on Nanotechnology-based Computing,*** October 21-22, 2022 Crete (Greece)**,** with the talk entitled *"Dependability Risks of Nanotechnology Based-Computing for Intelligent Systems"*

- **Invited Speaker** at *the* ***22ndAnnual Conference of the National Association of Risk Managers and Corporate Insurance Managers - ANRA,*** Milan (Italy), October 24-25, 2022, with the talk entitled "*Sfide per l'Affidabilità, la Safety e la Sicurezza di Sistemi Autonomi guidati da Intelligenza Artificiale*"

- **Invited Panelist** at the ***IEEE International Symposium on Technology and Society"***, panel entitled *"In celebration of SSIT's 50th Anniversary",* 10-12 November, 2022 (virtual)

- **Invited Speaker** at the ***IEEE Region 10 Humanitarian Technology Conference 2022,*** September 16-18, 2022, Hyderabad (India), with the talk entitled *"Safety, Reliability and Security Risks for Highly Autonomous Intelligent Systems"*

- **Invited Panelist** at the ***IEEE World Congress on Computational Intelligence - Industry Day,*** panel entitled *"Technological and Regulatory Challenges for AI in Europe"*, July 20, 2022, Padova (Italy)

- **Invited Panelist** at the Conference ***COMPSAC 2022,*** plenary panel entitled *"Reliability of Autonomous Machines",* online, June 27th – July 1st, 2022

- **Invited Panelist** at the Conference ***COMPSAC 2022,*** plenary panel entitled *"Technology Predictions",* online, June 27th – July 1st, 2022

- **Invited Talk** entitled *"Circuit Level Challenges and Solutions for Safe and Reliable Intelligent Systems"* at the ***ACM Workshop on Robustness and Safe Software 2.0 (RSS2) 2022,*** held online, February 28, 2022

- **Keynote Speaker** at ***The 15th IEEE International Conference on Application of Information and Communication Technologies (AICT2021),*** held online, October 13-15, 2021, with the talk entitled *"Safety, Reliability and Resiliency Challenges for Highly Autonomous Intelligent Systems"*

- **Keynote Speaker** at the ***4th International Conference on Recent Developments in Control Automation and Power Engineering (RDCAPE) 2021,*** October 7-8, 2021**,** held online, with the talk entitled *"Safety, Reliability and Resiliency Challenges to Enable a Smarter World"*

- **Keynote Speaker** at the ***31st International Conference on Field- Programmable Logic and Applications 2021,*** held online, September 1-3, 2021, with the talk entitled *"Safety, Reliability and Resiliency Challenges to Enable Highly Autonomous Intelligent Systems"*

- **Keynote Speaker** at the ***IEEE Computer Society Conference on Computers, Software and Applications (COMPSAC) 2021,*** held online, July 12-16, 2021, with the talk entitled *"Safety and Resiliency Challenges for Highly Autonomous Intelligent Systems"*

- **Invited Talk** entitled *"Safety and Reliability Challenges for Dependable Highly Autonomous Systems"* at ***IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT) 2021,*** held online, July 9-11, 2021

- **Invited Panel Moderator** at the Clust-ER Mech, Emilia Romagna (Italy) *Workshop* ***"La Guida Autonoma nella Auto e nei Veicoli per l'Agricoltura",*** held online, March 22, 2021

- **Invited Panelist** at the Conference ***COMPSAC 2021,*** plenary panel entitled *"President's Panel",* online, July 12-16, 2021

- **Invited Panelist** at the ***Singapore Week of Innovation & Technology (SWITCH) Conference*** panel entitled *"Technology Predictions for Times of Pandemics",* held online, December 7-11, 2020

- **Keynote Speaker** at the ***Applications in Electronics Pervading Industry, Environment and Society (APPLEPIES) 2020,*** held online, November 19-20, 2020, with the talk entitled *"Safety and Reliability Challenges to Enable a Smarter World"*

- **Invited Talk** entitled *"Safety and Reliability Challenges to Enable Highly Autonomous Intelligent Systems"* at ***IEEE CASS webinars,*** hosted by Rio Grande do Sul Chapter, held online, 6 November, 2020

- **Keynote Speaker** at the ***Women in Engineering Global Summit 2020,*** held online, November 5, 2020, with the talk entitled *"Reliability and Safety Challenges for Highly Autonomous Intelligent Systems"*

- **Invited Talk** held online, 17 October 2020, at the "***International Symposium on Frontiers Trends on Information and Computer Technology in Society" 2020, IEEE Indonesia Computer Society Chapter,*** with the talk entitled *"Being Part of the IEEE Computer Society in the Pandemic Emergency Year"*

- **Invited Talk** at the ***"Emergence of IEEE CS and Field of Computing in the past 7 Decades Curtain Raiser Meet at R10"***, held online, 10 October 2020, with the talk entitled *"Emergence of IEEE Computer Society in past 7 decades"*

- **Invited Panelist** at the Conference ***COMPSAC 2020*** plenary panel entitled *"To Patent or Not to Patent?"*, held Online, July 13-17, 2020

- **Distinguished Speaker** at the ***Women in Technology Forum*** of the **China National Computer Congress (*CNCC*) *2019,*** Suzhou (China), October 17-19, 2019, with the talk entitled *"Reliability and Safety Challenges for Autonomous Intelligent Systems with Intelligence at the Edge"*

- **Invited Welcome Message** at the ***China National Computer Congress (CNCC),*** Suzhou (China), October 17-19, 2019

- **Keynote Speaker** at the ***World Congress on Information Technology 2019,*** Yerevan (Armenia), October 6-9, 2019, with the talk entitled *"Reliability, Safety, Security and Time Determinism Challenges for Autonomous Intelligent Systems of a Smarter World"*

- **Invited Lecturer** at the ***Yerevan State University,*** Yerevan (Armenia), October 9, 2019, with the talk entitled *"Reliability and Safety Challenges in the IoT Era"*

- **Invited Talk** at ***Intel,*** Santa Clara (California), July 29, 2024, with the talk entitled *"Reliability, Safety and Security Risks due to Faults and Aging Phenomena affecting the AI Hardware"*

- **Invited Talk** at ***Synopsys,*** Yerevan (Armenia), October 9, 2019, with the talk entitled *"Addressed Challenges in Test, Reliability, Security and Energy Efficiency of Electronic Systems"*

- **Invited Talk** at ***Intel,*** Beijing (China), October 15, 2019, with the talk entitled *"Addressed Challenges in Test and Reliability of High Performance Electronic Systems"*

- **Invited Panelist** at the ***5th International Forum on Research and Technologies for Society and Industry 2019*** plenary panel entitled *"Be an entrepreneur in hot technological areas*", with the presentation entitled *"Hardware Information Processing Systems",* Florence (Italy), 9-12 Settembre, 2019

- **Invited Congress Opening Remarks** at the ***IEEE World Congress on Services 2019,*** Milan (Italy), 8-13 July, 2019

- **Invited Panelist** at the Conference ***COMPSAC 2019*** plenary panel entitled *"President's Panel: IEEE Computer Society Volunteerism & Membership – Serving Humanity with Technology"*, Milwaukee (USA), July 15-19, 2019

- **Invited Panelist** at the ***IEEE World Congress on Services 2019*** plenary panel entitled *"2020 Tech Predictions"*, Milan (Italy), 8-13 July, 2019

- **Invited Talk** at the ***Artemis Technology Conference 2019,*** Amsterdam (The Netherlands), 16-17 April 2019, with the talk entitled *"Reliability Challenges for Secure and Safe Cyber-Physical Systems and IoT Devices"*

- **Keynote Speaker** at the ***IPSJ's 81st National Congress***, Fukuoka (Japan), 14-16 March 2019, with the talk entitled *"Reliability Challenges for High Performance Microprocessors in the IoT Era"*

- **Invited Talk** at ***Yokohama Research Laboratory***, ***Hitachi,*** Yokohama (Japan), 13 March 2019, with the talk entitled *"Reliability Challenges for Microprocessors and Memories in the IoT Era"*

- **Keynote Speaker** at the ***IEEE Fruct Conference 2018,*** Bologna (Italy), November 14, 2018, with the talk entitled *"Reliability Challenges for High Performance Electronic Systems in the Internet of Things Era"*

- **Invited Talk** at ***Alibaba,*** Hangzhou (China), September 5, 2018, with the talk entitled: *"Reliability Challenges for Electronic Circuits and Systems in the Internet of Things Era"*

- **Invited Talk** at the ***Baidu ABC Summit,*** Shanghai (China), September 4, 2018, with the talk entitled: *"Reliability Challenges for Electronic Systems in the Big Data Era"*

- **Invited Talk** at **Baidu R&D Center,** Shanghai (China), September 4, 2018, with the talk entitled: *"Electronics' Reliability Challenges in the Internet of Things Era"*

- **Invited Talk** at the ***International Symposium on Future of Computer Technology 2018 (ISFCT2018),*** July 24, 2018, Tokyo (Japan), with the talk entitled: *"Reliability Challenges for High Performance Electronics in the Internet of Things Era"*

- **Invited Lecture** at the ***International PhD School***, ***University Federico II, Naples (Italy),*** June 19, 2018, with the lecture entitled: *"Reliability Challenges for VLSI Circuits and Systems"*

- **Invited Talk** at the ***SPS IPC Drivers 2017,*** May 24, 2017, Parma (Italy), with the talk entitled: *"Technologies for Big Data and Internet of Things"*

- **Keynote Speaker** with the talk entitles *"Test and Reliability Challenges for High Performance, Nanotechnology Circuits and Systems"*, at the ***IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS),*** Košice (Slovakia), April 20-22, 2016

- **Distinguished Lecturer** with the talk entitled ***"Test and Reliability Challenges for High Performance Circuits and Systems",*** at the ***48th Annual Meeting of the Associazione Gruppo Italiano di Elettronica,*** Brescia (Italy), June 22-24, 2016

- Invited Talk ***"Test and Reliability Challenges for Advanced Circuits and Systems",*** at the ***University of Padova (Italy),*** December 11, 2015

- Invited Talk ***"Test and Reliability Challenges of New Generation Circuits and Systems",*** at the ***University of Padova (Italy),*** December 5, 2014

- Invited Talk ***"Test and Reliability Challenges for High Performance Circuits and Systems",*** at the ***University of Padova (Italy),*** January 23, 2014

- **Invited Talk Speaker** at the ***3rd IEEE Workshop on Design for Reliability and Variability (DRV),*** Dana Point (California), May 4-5, 2011 with the talk entitled: *"Process Parameter and Clock Variations: How Can We Deal with Them in High Performance Microprocessors"*

- Invited Talk ***"Design for Testability and Reliability of High Performance Circuits and Systems",*** at the ***University of Padova (Italy),*** January 24, 2013

- Invited Talk at ***Hewlett-Packard,*** Palo Alto (CA, USA), December 7th, 2012, with the talk entitled: *"Fault-Tolerance for Highly Reliable Circuits and Systems"*

- Invited Talk at **3*SUN,*** Catania (Italy), September 8th, 2011, with the talk entitled: *"Faults and Fault-Tolerance for Photovolatic Systems"*

- Invited Talk at ***STMicroelectronics,*** Catania (Italy), September 8th, 2011, with the talk entitled: *"Fault and Degradation Modelling for Nanoscale ICs"*

- Invited Talk ***"Test and Reliability Challenges for General Purpose Nanoscale ICs",*** at the ***University of Padova (Italy),*** December 1, 2011

- **Invited Talk Speaker** at the ***IEEE East-West Design & Test International Symposium,*** St Petersburg (Russia), September 17-20, 2010 with the talk entitled: *"Secure Communication Protocol for Wireless Sensor Networks"*

- Invited Talk **entitled: *"On-Die Measurement of Process Parameter Variations and Clock Jitter",* at the "Elevator Talks" Session of the** *IEEE International Test Conference 2010,* **Austin (TX, USA),** October 31- November 5, 2010

- **Invited Talk Speaker** at the ***Workshop on Dependable and Secure Nanocomputing 2009 (WDSN09),*** Estoril (Portugal), June 29, 2009, with the talk entitled: *"Trading Off Dependability and Cost for Nanoscale High Performance Microprocessors: The Clock Distribution Problem*"

- **Invited Talk Speaker** at the ***IEEE East-West Design & Test International Symposium,*** Moscow (Russia), September 18-21, 2009 with the talk entitled: *"Dependable High Performance Microprocessors: The Clock Distribution Challenge"*

- **Invitation to serve as Invited Talk Speaker** at ***The IEEE International Workshop on Memory Technology, Design, and Testing (MTDT) 2009,*** Hsinchu (Taiwan), August 31 –September 2, 2009

- **Embedded Tutorial Speaker** at the ***NASA/ESA Conference on Adaptative Hardware and Systems (AHS-2009),*** San Francisco (California), July 29 – August 1, 2009, with the tutorial entitled: *"On-Die Calibration and Self-Correcting Approaches for Reliable Clock Distribution Networks of High Performance Microprocessors"* (together with Simon Tam and TM Mak, Intel Corporation)

- Invited Talk entitled *"Rad-Hard: Accurate Liner Model for SET Critical Charge Estimation",* at ***ST Microelectronics,*** Catania (Italy), September 14th, 2010

- Invited Talk entitled: *"Low-Cost Control-Oriented Concurrent Error Detection Schemes for RAS, Debug and Test",* at ***Intel Corporation,*** Santa Clara (CA), February 27th, 2009

- Invited Talk ***"Design and Test Challenges for General Purpose Nanoscale Systems",*** at the ***University of Padova (Italy),*** November 25, 2009

- Invited Talk entitled: ***"****Soft Errors: Risks and Remedies for Next Generation ICs",* at ***CISCO,*** **San Josè (CA),** February 25th, 2009

- Invited Talk *"IC Design and Testing Challenges with Technology Scaling",* at the ***University of Padova (Italy),*** November 13, 2008

- Invited participation to the ***"****European Research, Innovation & Competitiveness",* ***European Parliament,*** Brussel (Belgium), January 28, 2009

- Invited Talk entitled: *"New Low Cost Approach for High Performance Microprocessor Concurrent Error Detection",* at the "Elevator Talks" Session of the ***IEEE International Test Conference 2008,*** Santa Clara (CA, USA), October 29th, 2008

- Invited Talk entitled *"Fault Tolerance and Hardening Approaches to Protect Logic Against Clock Faults and Soft Errors",* at ***IBM, Poughkeepsie-New York (USA),*** September 26th, 2008

- Invitation to participate to the ***"Intel European Research and Innovation Conference 2008",*** organized by ***Intel Education***, Dublin (Irland), September 10-12, 2008

- Invited Talk entitled *"Scaling of Microelectronic Technology: Testing and Design For Testability Challenges for Digital Electronic Circuits ",* at the ***University of Padova (Italy),*** November 26, 2007

- Invited Talk entitled *"Testing e Design For Testability di Circuiti Elettronici Digitali",* at the ***University of Padova (Italy),*** November 30, 2006

- Invited Talk entitled *"Collaudo e Progettazione Orientata al Collaudo di Sistemi Elettronici Digitali",* at the ***University of Padova (Italy),*** December 1st, 2005

- Invited Talk entitled: "*Potentials of Fault Tolerance Paradigms for Scaled ICs' Faults*", at ***Intel Corporation, Santa Clara (CA),*** August 6th, 2004

- Invited Tutorial on *"Testing and Fault Tolerance",* at ***STMicroelectronics (Switzerland),*** April 6th, 2004

- Invited Talk entitled: ***"****Testing Clock Faults: Those That We Might Have Missed",* at ***Intel Corporation,*** Santa Clara (CA), December 8th, 2004

- Invited Talk entitled *"Can High Performance Be Achieved Without Reliability Risks ?"* at ***Philips Research Labs.,*** Eindhoven (The Netherlands), March 17th, 2003

- Invited Talk entitled *"Will Soft Errors Become a Problem and How Could We Solve It ?",* ***Intel Corporation (MA),*** November 6th, 2003

- Invited Talk entitled *"Faults on the Clock Distribution Network and Their Impact on Testing"* at ***Artisan Components,*** Sunny Valley (CA, USA), November 21st, 2002

- Invited Talk entitled *"Hardware Solutions for the Concurrent Detection of Transient, Crosstalk and Delay Faults in VDSM ICs"* at ***Agere Systems,*** Murray Hill (NJ, USA), May 17, 2001

- Invited Talk entitled *"On-Line Testing for Logic Soft Errors: A Better Way",* at the ***Intel Test Research Symposium,*** Intel, Santa Clara (CA), September 29th, 2000

- Invited Tutorial entitled *"Hardware Fault-Tolerance: New Perspectives for Very Deep Sub-Micron Circuits ?",* at ***ST Microelectronics,*** Agrate (Milan, Italy), July 10th, 2000

- Invited Talk entitled *"Soft Errors' On-Line Testing: A Low Cost Approach",* at ***LogicVision,*** San Josè (CA), September 28th, 2000

- Invited Talk entitled *"Concurrent Testing Techniques for Clock's Faults",* at the ***Intel Research Symposium VLSI Test, Intel,*** Santa Clara (CA), April 24th, 1998

- Invited Talk entitled *"Self-Checking Detectors for Faults Escaping Conventional Off-Line and On-Line Testing",* at ***The Boeing Company,*** Seattle (USA), October 27, 1998

- Invited Lesson entitled *"Checker Design",* at the ***"European School on High Reliability Integrated Systems", Euroform,*** Bologna, February 9th, 1994

- Invited Lessons on *"Reliability and Diagnostics",* at the ***Corso di Perfezionamento Post-Laurea*** **of the *CEFRIEL,*** Politecnico of Milan, June 4-5, 2002

- **Panelist** for the panel entitled: "Innovation & Cooperation in Europe", of the **"14th European Manufacturing Test Conference (EMTC), Semicon Europa",** 9-11 October, 2012, Dresden (Germany), organized by R. Segers, *ReSeCo (The Netherlands)*

- **Panelist** for the panel entitled: *"How can defect-based test be made to work in a foundry world?",* of the ***IEEE International On-Line Testing Symposium,*** 7-9 July, 2003, Kos (Greece), organized by R. Aitken, *Artisan Components (USA)*

- **Panelist** for the panel entitled: *"Mainframe RAS on Desktops : Reality today or tomorrow"*, of ***The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems,*** Rome (Italy), September 26-28, 2007, organized by Prashant D. Joshi, *Intel*

Research Contracts' Responsibility and Scientific Collaborations

- **Responsible** of the *Consultancy Contract* with ***Beghelli Spa (Bologna)*** for the project *"Sicurlume"* funded by the *Italian Ministry for Economic Development*, 2023-2025

- **Responsible** for the *safety part* of *the Consultancy Contract* with ***Thales Italia Spa*** for the project *"ILS Distribuito"* funded by the *Italian Ministry for Economic Development*, 2023-2025

- **Participant** to the *Italian National Center on High Performance Computing, Big Data e Quantum Computing* (September 2022 - August 2025),

- **Participant** to the *Italian Research Project on Security and Rights In the CyberSpace – SERICS* (January 2023 - December 2025).

- **Recipient** of a *Research Grant* from ***Intel Corporation,*** for researches on *"Check the Checker Approaches for High Performance Microprocessors of Autonomous Systems"*, May 2020 – April 2021

- **Recipient** of a *Research Grant* from ***Intel Corporation,*** for researches on *"Power Faults On-Line Detection and Reaction in Complex SoCs"*, October 2018 - September 2019

- **Responsible** of the *"Luminare" Research Contract* with ***Becar-Beghelli (Bologna)*** funded by the *Italian Ministry for Economic Development*, September 2017 - 2019

- **Responsible** of a *Research Contract* with ***Intel Corporation (Santa Clara, CA),*** for researches on "*Techniques to Control PowerDroop/Activity Factor During Logic BIST"*, November 2014-2015

- **Responsible** of a *Research Contract* with ***Intel Corporation (Santa Clara, CA),*** for researches on "*Techniques to Control PowerDroop/Activity Factor During Logic BIST"*, November 2013-2014

- **Responsible** of a *Research Contract* with ***Intel Corporation (Santa Clara, CA),*** for researches on "*Techniques to Control PowerDroop/Activity Factor During Logic BIST"*, November 2012-2013

- **Responsible** of a *Research Contract* with ***Intel Corporation (Santa Clara, CA),*** for researches on "*Techniques to Control PowerDroop/Activity Factor During Logic BIST"*, November 2011-2012

- **Recipient** of a *Cash Grant (in lieu of equipment)* from ***Intel Corporation (Santa Clara, CA),*** October 2008

- **Responsible** of a *Research Contract* with ***Becar-Beghelli (Bologna)*** on the *:"Study of a Protocol for the Security of the Information Transmitted on a Proprietary Wireless Network"*, funded by the *Italian Ministry for Economic Development*, November 2008 - October 2009

- **Responsible** of the Bologna Unit for a 2008-2009 PRIN project funded by the **Italian Ministry MIUR**

- **Recipient** of a *Research Grant* from ***Intel Corporation (Santa Clara, CA),*** for researches on "*Clock Fault Testing and DFT"*, July 2008- June 2009

- **Recipient** of a *Research Grant* from ***Intel Corporation (Santa Clara, CA),*** for researches on *"Low Cost Control Logic Concurrent Error Detection Schemes for RAS, Debug and Test"*, May 2007- September 2009

- **Recipient** of a *Research Grant* from ***Intel Corporation (Santa Clara, CA),*** for researches on "*Clock Fault Testing and DFT"*, May 2006- April 2008

- **Responsible** for the Research Contract with ***Intel Corporation (Hillsboro, Oregon)*** entitled: *"Development of Optimal Error Correcting Codes for Caches"*, January – September 2006

- **Recipient** of a *Research Grant* from ***Intel Corporation (Santa Clara, CA),*** for researches on *"DFT for Detection of Clock Distribution Faults",* January- December 2005

- **Recipient** of a *Research Grant* from ***Intel Corporation (Santa Clara, CA),*** for researches on *"DFT for Detection of Clock Distribution Faults",* January- December 2004

- **Recipient** of an *Equipment Grant* from ***Intel Corporation (Santa Clara, CA),*** 2004

- **Responsible** for the Research Contract with ***STMicroelectronics*** entitled: *"Modelling, Analysis and Fault Tolerance of Interconnects Among Different Cores of Systems in Package"*, January-December 2006

- **Responsible** for the Research Contract with ***STMicroelectronics*** entitled: *"Design and Testing Paradigms for Reliable Multiprocessor Systems"*, 2004-2006

- **Responsible** of the Bologna Unit for a Research Contract funded by ***the Italian Space Agency*** (ASI) 2005-2006

- **Responsible** of the Bologna Unit for a 2004-2005 PRIN project funded by the **Italian Ministry MIUR**

- **Responsible** of the Bologna Unit for the European Project (n. IST-2001-38782) funded by the **European Community** within the Fifth Framework Programme entitled: *"Fault Tolerance: Electrical Aspects"*, coordinated by ***Philips Research Labs.,*** Eindhoven (The Netherlands), 2003-2004

- **Responsible** of the Bologna Unit for the Research Contract funded by ***the Italian Space Agency*** (ASI) entitled: *"Definition and Development of Techniques for the Identification and Tolerance of Faults for the Design of Computing Systems Based on Programmable Logic Devices",* 2000-2002

- **Responsible** for the Research Contract with ***STMicroelectronics*** entitled: *"Design and Communication Paradigms for Reliable Automata Systems"*, 2000-2003

- **Responsible** for the Research Contract with ***Alstom Transport*** entitled: *"Controller of TFM Self-Checking Protocol Implemented by Field Programmable Gate Array (FPGA) Technology",* 2001-2002

- **Responsible** for the Research Contract with ***Alstom Transport*** entitled*: "System for the Functional Verification of Electronic Control Systems of Railway Stations"*, 2002-2003

- **Responsible** of *Scientific Collaborations* with the ***Institute of Astrophysics and Cosmic Physic*** **of the *Italian National Research Council*** (Milan, Italy)

- **Responsible** of *Scientific Collaborations* with the ***Northeastern University,*** Boston (MA, USA)

- **Responsible** of *Scientific Collaborations* with the ***Georgia Tech University,*** Atlanta (Georgia, USA)

- **Responsible** of *Scientific Collaborations* with the ***Simon Fraser University,*** Vancouver (BC, Canada)

- **Responsible** of *Scientific Collaborations* with the ***Linköpings University,*** Linköpings (Sweden)

- **Responsible** of *Scientific Collaborations* with the ***Stuttgart University,*** Stuttgart (Germany)

Grants

- Grant from the *National Research Council* (Italy) - 1997

- Post PhD Grant from the *University of Bologna* (Italy) - 1996

- Grant from the *National Research Council* (Italy) - 1995

- PhD Grant from the *University of Bologna* (Italy) - 1992

- Grant from the *National Research Council* (Italy) - November 1991

- Grant from *SGS-Thomson* (Milan, Italy) - May 1991

Courses Taught

- (Graduate) course ***"Reliable Data Processing and Storage for Intelligent Systems M"*** for the Magistral Laurea Degree in Electronic technologies for Big data and Internet of Things (E-BIT) of the ***University of Bologna*** for the Academic Year 2020-2021, 2021-2022, 2022-2023, 2023-2024, 2024-2025

- (Graduate) course ***"Design for Reliable Data Processing and Storage M"*** for the Magistral Laurea Degree in Electronic technologies for Big data and Internet of Things (E-BIT) of the ***University of Bologna*** for the Academic Year 2017-2018, 2018-2019, 2019-2020

- (Graduate) course ***"Test, Diagnosis and Reliability M"*** for the Magistral Laurea Degree in Advanced Automotive Electronic Engineering (A2E2) of the ***University of Bologna, University of Modena e Reggio Emilia, University of Parma, University of Ferrara*** for the Academic Year 2017-2018, 2018-2019, 2019-2020, 2020-2021, 2021-2022, 2022-2023, 2023-2024 (Module 1), 2024-2025 (Module 1)

- Coordination for the (Graduate) course ***"Trends in Electronics M"*** for the Magistral Laurea Degree in Electronics and Communications Science Technology of the ***University of Bologna*** for the Academic Year 2016-2017, 2017-2018

- Coordination for the (Graduate) course ***"Industrial Trends in Electronics M"*** for the Magistral Laurea Degree in Electronics and Communications Science Technology of the ***University of Bologna*** for the Academic Year 2018-2019, 2019-2020, 2020-2021, 2021-2022, 2022-2023

- (Graduate) course ***"High Reliability Electronics Systems M"*** for the Magistral Laurea Degree in Electronic Engineering of the ***University of Bologna*** for the Academic Year 2010-2011, 2011-2012, 2012-2013, 2013-2014, 2014-2015, 2015-2016, 2016-2017, 2017-2018, 2018-2019, 2020-2021

- (Graduate) course ***"High Reliability and Resiliency Electronics Systems M"*** for the Magistral Laurea Degree in Electronic Engineering of the ***University of Bologna*** for the Academic Year 2021-2022, 2022-2023, 2023-2024, 2024-2025

- (Graduate) course ***"Design for Testability and Reliability of Integrated Circuits M"*** for the Magistral Laurea Degree in Electronics and Communications Science Technology of the ***University of Bologna*** for the Academic Years: 2009-2010, 2010-2011, 2011-2012, 2012-2013, 2013-2014, 2014-2015, 2015-2016, 2016-2017

- (Graduate) course ***"Lab of Reliable Systems Design M"*** for the Magistral Laurea Degree in Electronic Engineering of the ***University of Bologna*** for the Academic Years: 2014-2015, 2015-2016, 2016-2017, 2017-2018, 2018-2019, 2019-2020

- (Graduate) course ***"Lab of Reliable Intelligent Systems M"*** for the Magistral Laurea Degree in Electronic Engineering of the ***University of Bologna*** for the Academic Year 2020-2021, 2021-2022, 2022-2023, 2023-2024, 2024-2025

- (Undergraduate) course ***"Electronics T"*** for the Laurea Degree in Electrical Engineering of the ***University of Bologna*** for the Academic Years: 2009-2010, 2010-2011

- (Graduate) course ***"High Reliability Electronics Systems LS"*** for the Specialistic Laurea Degree in Electronic Engineering of the ***University of Bologna*** for the Academic Years: 2002-2003, 2003-2004, 2004-2005, 2005-2006, 2006-2007, 2007-2008, 2008-2009

- (Undergraduate) course ***"Electronics L"*** for the Laurea Degree in Electrical Engineering of the ***University of Bologna*** for the Academic Years: 2006-2007, 2007-2008, 2008-2009

- (Undergraduate) course ***"Digital Electronics"*** for the Laurea Degree in Computer Science Engineering of the ***University of Bologna*** for the Academic Year 2005-2006

- (Undergraduate) course ***"Digital Electronics"*** for the Laurea Degree in Computer Science Engineering of the ***University of Bologna*** for the Academic Year 2004-2005

- (Undergraduate) course ***"Analog Electronics"*** for the Laurea Degree in Computer Science Engineering of the ***University of Bologna*** for the Academic Year 2003-2004

- (Graduate) course ***"Reliability and Diagnosis of Electronic Components and Circuits - Module I and Module II"*** for the Degree in Electronic Engineering of the ***University of Bologna*** for the Academic Year 2002-2003

- (Graduate) course ***"Reliability and Diagnosis of Electronic Components and Circuits - Module I"*** for the Degree in Electronic Engineering of the ***University of Bologna*** for the Academic Year 2001-2002

- (Undergraduate) course ***"Applied Electronics"*** for the Degree in Engineering for the Environment and Resources of the ***University of Bologna*** for the Academic Years: 1998-1999, 1999-2000, 2000-2001, 2001-2002

- (Undergraduate) course ***"Automatic Design of Electronic Circuits and Systems"*** for the degree in Electronic Engineering of the ***University of Udine*** for the Academic Year 1995-1996

Academic Responsibilities

- (September 2023) **Elected President of the School of Engineering** of the *University of Bologna*

- (From the A.A. 2018-19 to September 2023) **Deputy-President of the School of Engineering** of the *University of Bologna*

- (From the A.A. 2016-2017 to the A.A. 2021-2022) **Coordinator of the Master Curricula in Electronic Engineering** of the *School of Engineering and Architecture of the University of Bologna*

- (2020-2021) Appointment as an expert within the **Gruppo di Esperti della Valutazione (GEV)** for the evaluation of the research quality (VQR) 2015-2019, **Agenzia Nazionale di Valutazione del Sistema Universitario e della Ricerca (ANVUR)**

- (2016-2018) **Member of the Funding Committee** of the *School of Engineering and Architecture of the University of Bologna*

- (2015) **Reviewer** for the applications to the *New Position of Full Professor* for Computer Architecture at the Faculty of Informatics at the **Vienna University of Technology (TU Wien).**

- (2015) **External Reviewer** for the *Promotion Review Process* for promotion to the rank of *Full Professor* in the area of Information Technology at the **United Arab Emirates University (UAEU)**

- (2018) **Member** of the Evaluation Committee for the selective procedure for a position of *Professor di Seconda Fascia* of the **University of Pavia (Italy).**

- (2017) **Member** of the Evaluation Committee for the selective procedure for a position of *Professor di Seconda Fascia* of the **University of Bologna (Italy).**

- (2017) **Member** of the Evaluation Committee for the selective procedure for a position of *Professor di Prima Fascia* of the **University of Parma (Italy).**

- (2017) **Member** of the Evaluation Committee for the selective procedure for a position of *Professor di Seconda Fascia* of the **University of Torino (Italy).**

- (2016) **Member** of the Evaluation Committee for the selective procedure for a position of *Professor di Seconda Fascia* at the **University of Bergamo (Italy).**

- (2015) **Member** of the Evaluation Committee for the selective procedure for a position of *Professor di Prima Fascia* at the **University of Trento (Italy).**

- (2014) **Member** of the Evaluation Committee for the selective procedure for a position of *Researcher RTdB* at the **University of Padova (Italy).**

- (July 2013-2022) **President** of the *Commissione per la Valutazione* of the curricula of the candidates for the role of ***Contract Professor*** and of the candidates for the role of ***Contract Tutor*** for the courses of the ***Laurea and Laurea Magistrale*** of the School of Engineering and Architecture – Bologna and Ravenna in "Electrical, Electronic and Measure Engineering"

- (June 2013 - December 2015) **Member of the Census Commission** of the *School of Engineering and Architecture of the University of Bologna*

- (November 2017) **External Member** of the **Examination Commission of the defence** for the **PhD in Technical Sciences (Dr. techn.)** of the **Technischen Universität, Wien (Austria)** of Savulimedu Veeravalli, PhD thesis entitled: *"Design of Custom ASIC for Radiation Experiments to Study Single Event Effects"*

- (2024) **Member of the Board of Examiners** for the final oral defence of a PhD candidate at the *Politecnico di Torino*

- (2015) **Member of the Board of Examiners** for the final oral defence of PhD candidates of the *Scuola Interpolitecnica di Dottorato (Politecnico di Torino, Politecnico di Milano, Politecnico di Bari)* – "Information and Communication Technologies" Area

- (2013-2014) **Member of the Board of Experts** of the *Italian University and Research Ministry (MIUR)*

- (October 2009-2012) **Member (Elected) of the Board of the Department of Electronics, Informatics and Systems (DEIS)** of the ***Engineering Faculty*** *of the University of Bologna*

- (October 2009) **External Member** of the **Examination Commission of the defence** for the **PhD in Technical Sciences (Dr. techn.)** of the **Technischen Universität, Wien (Austria)** of Gottfried Fuchs, PhD thesis entitled: *"Fault Tolerant Distributed Algorithms for On-Chip Tick Generation: Concepts, Implementations and Evaluations"*

- (October 2009) **Member of the Examination Commission for the admission** to the **PhD Course in "Information Technologies"** *of the University of Bologna*, ARCES

- (2009-2010) **Member of the Examination Commission of the defence** for the **PhD in "Electronic, Computer Science and Telecommunication Engineering"** *of the University of Bologna*, DEIS

- (2009-2010) **External Member of the Examination Commission of the defence** for the **PhD in "Information Engineering"** o*f the University of Padova (Italy)*

- (2009-2012) **Member of the Professor Committee** for the **PhD in "Information Technologies"** *of the University of Bologna*, ARCES

- (2007) **President of the Evaluation Commission n. II** of the ***Engineering Faculty*** *of the University of Bologna f*or the ***National State Exams for Professional Engineering Qualification***

- (2007-2012) **Member (Elected) of the Funding Committee** of the ***Engineering Faculty*** *of the University of Bologna*

- (2003-2008) **Responsible of student curricula** for the ***Electronic Engineering Faculty*** of the *University of Bologna*

Organization, Direction and Coordination of Research Groups

- **Supervision of Assistant Professor Research Projects:**

  - **Supervisor** of the **Collaboration Project (**on *"Circuit Reliability, Fault Tolerance, and On-Line Error Detection and Correction"***)** with Jennifer Dworak, **Assistant Professor, Brown University (USA),** within the *Career Development Award of NSF (USA)*

- **Funding/Supervision of Research Associates:**

  - **Dr. Eng. Daniele Rossi,** DEIS – Research Associate at the Department of Electronics, Informatics and Systems (DEIS) of the University of Bologna, 2005-2014 (funded/co-funded by industrial research projects for which C. Metra is/has been responsible)

- **Dr. Eng. Martin Omaña,** DEIS – Research Associate at the Department of Electronics, Informatics and Systems (DEIS) of the University of Bologna, since 2006 (funded/co-funded by industrial research projects for which C. Metra is/has been responsible)

- **Funding/Supervision of PhD Students:**

  - **Eng. Matteo Naldi,** PhD student at University of Bologna, November 2022 – October 2025 (funded by STMicroelectronics)

  - **Eng. Zahra Shirmohammadi,** PhD student at University of Technology, Tehran (Iran), September 2016 – June 2017

  - **Eng. Meryem Bouras,** PhD student at Mohammed V University in Rabat, Rabat (Marocco), September 2016 - June 2017

  - **Eng. Vimalathithan Rathinasabapathy,** PhD student at Anna University, Coimbatore (India), September 2010 – July 2011

  - **Eng. Daniele Giaffreda,** ARCES – University of Bologna, **XXV cycle of the PhD Course,** January 2010 – August 2011 (co-funded by industrial research projects for which C. Metra is/has been responsible)

  - **Eng. Daniele Rossi,** DEIS – University of Bologna, XVII cycle of the PhD Course (PhD funded by industrial research projects for which C. Metra was responsible)

  - **Eng. Martin Omaña,** DEIS - University of Bologna, XVII cycle of the PhD Course

  - **Eng. Josè Manuel Cazeaux** - DEIS - University of Bologna, XVIII cycle of the PhD Course

  - **External reviewer for the Ph.D.** in Computer Science of the University of Verona (Italy) of A. Fin, entitled *"A Functional Testing Framework for Embedded Systems"*

- **Funding and/or Supervision of Research Grant Recipients/Collaborators:**

  - **Eng. Andrea Pagano,** Research Grant Recipient at the Department of Electronics, Informatics and Systems (DEIS) of the University of Bologna, 2001, funded/co-funded by industrial research projects for which C. Metra was responsible

  - **Eng. Luca Schiano,** Research Grant Recipient at the Department of Electronics, Informatics and Systems (DEIS) of the University of Bologna, 2001-2002, funded/co-funded by industrial research projects for which C. Metra was responsible

  - **Eng. Stefano Di Francescantonio,** Research Grant Recipient at the Department of Electronics, Informatics and Systems (DEIS) of the University of Bologna, 2001 – 2003, funded/co-funded by industrial research projects for which C. Metra was responsible

- **Dr. Ing. Martin Omaña,** Research Collaborator at the Department of Electronics, Informatics and Systems (DEIS) of the University of Bologna, 2005, funded/co-funded by industrial research projects for which C. Metra was responsible

- **Eng. Óscar Ariño Zorilla (Spain), "**Leonardo da Vinci Program" Grant Recipient at the *Advanced Research Centre on Electronic Systems for Information and Communication Technologies E. De Castro (ARCES)* of the Univ. of Bologna

- **Eng. Sara Cretì,** Research Grant Recipient at the Department of Electronics, Informatics and Systems (DEIS) of the University of Bologna, September 2023 – August 2024, funded by the Italian National Research Center on High Performance Computing, Big Data and Quantum Computing

- **Supervision of Laurea Degree Thesis:**

  - **Supervisor** for numerous thesis for the **Laurea Degree in Electronic Engineering** of the University of Bologna (Italy), some of which in collaboration with industries (e.g., Intel Corporation, Maserati, Toyota, Electrolux, ABB EVI, Alstom Transport, STMicroelectronics, Becar-Beghelli, etc.)

Publications

Refereed International Journals/Books

1. **C. Metra**, B. Riccò, "Enhanced reliability evaluation for self-checking circuits", in *IEE Electronics Letters*, Vol. 30, No. 10, pp.776–778, 12 May, 1994, Institution of Electrical Engineers, Stevenage SG1 2AY (United Kingdom), 1994.
2. **C. Metra**, M. Favalli, B. Riccò, "Novel 1-out-of-n CMOS checker", in *IEE Electronics Letters*, Vol. 30, No. 17, pp. 1398–1400, 18 August, 1994, Institution of Electrical Engineers, Stevenage SG1 2AY (United Kingdom), 1994.
3. **C. Metra**, M. Favalli, B. Riccò, "Design of CMOS self-checking sequential circuits with improved detectability of bridging faults", in *IEE Electronics Letters*, Vol. 30, No. 23, pp. 1934–1936, 10 November, 1994, Institution of Electrical Engineers, Stevenage SG1 2AY (United Kingdom), 1994.
4. **C. Metra**, "Circuiti CMOS Self-Checking" (Tesi di Dottorato), Bologna, Febbraio 1994.
5. **C. Metra**, M. Favalli, P. Olivo, B. Riccò, "Design of CMOS Checkers with Improved Testability of Bridging and Transistor Stuck-on Faults", in *Journal of Electronic Testing: Theory and Applications (JETTA)*, Vol. 6, No. 1, pp. 7–22, February 1995, Kluwer Academic Publishers, Norwell, MA 02061 (USA), 1995.
6. **C. Metra**, M. Favalli, B. Riccò, "Design of TSC CMOS Checkers for Any 1-out-of-n Code", in *Journal of Microelectronic Systems Integration*, Vol. 3, No. 2, pp. 109–120, 1995, Plenum Publishing Corporation, New York (USA), 1995.

7. **C. Metra**, M. Favalli, "1-out-of-n dynamic CMOS checker", in *IEE Electronics Letters*, Vol. 31, No. 23, 9 November, pp. 1999-2000, 1995, Institution of Electrical Engineers, Stevenage SG1 2AY (United Kingdom), 1995.
8. M. Favalli, **C. Metra**, "Sensing circuit for on-line detection of delay faults", in *IEEE Transactions on VLSI Systems*, Vol. 4, No. 1, pp. 130-133, March 1996, The Institute of Electrical and Electronics Engineers Inc., Piscataway, (NJ), 1996.
9. M. Favalli, **C. Metra**, "Design of low-power CMOS two-rail checkers", in *Journal of Microelectronic Systems Integration*, Vol. 5, No. 2, pp. 101–110, 1997, Plenum Publishing Corporation, New York (USA), 1997.
10. **C. Metra**, M. Favalli, B. Riccò, "1-out-of-3 Code Checker with Single Output", in *IEE Electronics Letters*, Vol. 33, No. 16, 31 July, pp. 1373-1374, 1997, Institution of Electrical Engineers, Stevenage SG1 2AY (United Kingdom), 1997.
11. **C. Metra**, M. Favalli, P. Olivo, B. Riccò, "On-Line Detection of Bridging and Delay Faults in Functional Blocks of CMOS Self-Checking Circuits", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (CAD/ICAS)*, Vol. 16, No. 7, July, pp. 770-776, 1997, The Institute of Electrical and Electronics Engineers Inc., Piscataway, (NJ), 1997.
12. **C. Metra**, M. Favalli, B. Riccò, "On-Line Self-Testing Voting and Detecting Schemes for TMR Systems", in *Journal of Microelectronic Systems Integration*, Vol. 5, No. 4, pp. 261–273, 1997, Plenum Publishing Corporation, New York (USA), 1997.
13. **C. Metra,** "Design Technique for Embedded 1-out-of-3 Checkers", in *Alta Frequenza Rivista di Elettronica*, Vol. 9, No 2, pp. 68-70, 1997, Associazione Elettrotecnica ed Elettronica Italiana, Milano, 1997.
14. **C. Metra,** M. Favalli, B. Riccò, "Concurrent Checking of Clock Signals' Correctness", in *IEEE Design* & *Test of Computers*, Vol. October - November, pp. 42–48, 1998, IEEE Computer Society Press, Los Alamitos (California), 1998.
15. **(Invited Paper) C. Metra,** "Majority Logic", in *Wiley Encyclopedia of Electrical and Electronics Engineering*, Vol. 12, pp. 317--322, February 1999, Wiley & Sons., Inc., Publishers, New York (USA), 1999.
16. (Invited conference report) **C. Metra**, Neil Harrison, "DFT Symposium 98", in *IEEE Design & Test of Computers*, Vol. January-March, p. 5, 1999, IEEE Computer Society Press, Los Alamitos (California), e in *The Newsletter of the Test Technology Technical Council of the IEEE Computer Society*, Amissville, VA 937-7848 (USA), 1999.
17. M. Favalli, **C. Metra**, "Bus Crosstalk Fault Detection Capabilities of Error Detecting Codes for On-Line Testing", in *IEEE Transactions on VLSI Systems*, Vol. 7, No. 3, pp. 392–396, Settembre, 1999, The Institute of Electrical and Electronics Engineers Inc., Piscataway, (NJ), 1999.
18. (Invited conference report) **C. Metra**, Neil Harrison, "Defect and Fault Tolerance Symposium 1999", in *Test Technology Newsletter - The Newsletter of the Test Technology Technical Council of the IEEE Computer Society*, October-December, 1999, TTTC Office, 1474 Freeman Drive, Amissville, VA 20106 (USA), 1999.
19. **C. Metra,** M. Favalli, B. Riccò, "Signal Coding and CMOS Gates for Combinational Functional Blocks of Very Deep Submicron Self-checking Circuits", in *VLSI Design*, Vol. 11, No. 1, 2000, pp. 23–34, OPA N.V., published by licence under the Gordon and Breach Science (ISSN: 1065-514X), Newark, NJ 07102, printed in Malaysia, 2000.
20. **C. Metra**, M. Favalli, B. Riccò, "Self-Checking Detection and Diagnosis Scheme for Transient, Delay and Crosstalk Faults Affecting Bus Lines", in *IEEE Transactions on Computers*, Vol. 49, No. 6, June 2000, pp. 560–574, IEEE Computer Society Press, Los Alamitos (California), 2000

21. M. Favalli, **C. Metra**, "Bridging Faults in Pipelined Circuits", in *Journal of Electronic Testing: Theory and Applications*, Vol. 16, Issue 6, December 2000, pp. 617—629, Kluwer Academic Publishers, Norwell, MA 02061 (USA), 2000.
22. **C. Metra**, J-C. Lo, "Intermediacy Prediction for High Speed Berger Code Checkers", in *Journal of Electronic Testing: Theory and Applications*, Vol. 16, Issue 6, December 2000, pp. 607–615, Kluwer Academic Publishers, Norwell, MA 02061 (USA), 2000.
23. Lombardi, **C. Metra**, "Defect-Oriented Diagnosis for Very Deep-Submicron Systems", in *IEEE Design & Test of Computers*, **V**ol. January-February, pp. 8–9, 2001, IEEE Computer Society Press, Los Alamitos (California), 2001.
24. **C. Metra**, B. Riccò, "Soluzioni Hardware per Sistemi Integrati Digitali ad Alta Sicurezza", in *Alta Frequenza Rivista di Elettronica*, Vol. 13, No 3, pp. 4-10, Maggio-Giugno 2001, Associazione Elettrotecnica ed Elettronica Italiana, Milano, 2001.
25. Favalli, **C. Metra**, "On-Line Testing Approach for Very Deep-Submicron ICs", in *IEEE Design & Test of Computers*, Vol. March-April, 2002, pp. 16—23, IEEE Computer Society Press, Los Alamitos (California), 2002.
26. D. Nikolos, J. Hayes, M. Nicolaidis, **C. Metra**, "Guest Editorial of the Special Issue on the 7th IEEE International On-Line Testing Workshop", in *The Journal of Electronic Testing: Theory and Applications (JETTA),* Vol. 18, n. 3, pp. 259--260, June 2002, Kluwer Academic Publishers, Norwell, MA 02061 (USA), 2002.
27. M. Favalli, **C. Metra,** "Single output distributed two-rail checker with diagnosing capabilities for bus based self-checking architectures", in *Journal of Electronic Testing: Theory and Applications,* Vol. 18, n. 3, pp. 273-283, June 2002, Kluwer Academic Publishers, Norwell, MA 02061 (USA), 2002.
28. **C. Metra**, M. Favalli, S. Di Francescantonio, B. Riccò, "On-Chip Clock Faults' Detector", in *The Journal of Electronic Testing: Theory and Applications (JETTA),* Vol. 18, n. 4, pp. 555-564, August, 2002, Kluwer Academic Publishers, Norwell, MA 02061 (USA), 2002.
29. **C. Metra,** S. Di Francescantonio, M. Favalli, B. Riccò, "Scan Flip-Flops with On-Line Testing Ability with respect to input Delay and Crosstalk Faults", in *Microelectronics Journal,* Vol. 34, n. 1, pp. 23-29, January, 2003, Elsevier Science (ISSN 0026-2692).
30. **C. Metra**, M. Sonza Reorda, "Guest Editorial", in *The Journal of Electronic Testing: Theory and Applications (JETTA),* Vol. 19, No. 5, October 2003, p. 499, Kluwer Academic Publishers, Norwell, MA 02061 (USA), 2003.
31. D. Rossi, **C. Metra**, "Error correcting strategy for high speed and density reliable flash memories", in *The Journal of Electronic Testing: Theory and Applications (JETTA),* Vol. 19, No. 5, October 2003, pp. 511-521, Kluwer Academic Publishers, Norwell, MA 02061 (USA), 2003.
32. L. Schiano, **C. Metra**, D. Marino, "Self-Checking Design, Implementation and Measurement of a Controller for Track-Side Railway Systems", in *IEEE Transactions on Instrumentation and Measurement,* Vol. 52, No. 6, pp. 1722—1728, December 2003, The Institute of Electrical and Electronics Engineers Inc., Piscataway, (NJ), 2003.
33. **C. Metra**, L. Schiano, M. Favalli, "Concurrent Detection of Power Supply Noise", in *IEEE Transactions on Reliability,* Vol. 52, No. 4, pp. 469—475, December 2003, The Institute of Electrical and Electronics Engineers Inc., Piscataway, (NJ), 2003.
34. A. Ivanov, F. Lombardi, **C. Metra**, "Guest Editors' Introduction: Advances in VLSI Testing at MultiGbps Rates", in *IEEE Design & Test of Computers*, Vol. July-August, 2004, pp. 274—276, IEEE Computer Society Press, Los Alamitos (California), 2004.
35. **C. Metra,** S. Di Francescantonio, TM Mak, "Implications of Clock Distribution Faults and Issues with Screening Them During Manufacturing Testing", in *IEEE Transactions on Computers,* Vol. 53, No. 5, May 2004, IEEE Computer Society Press, Los Alamitos (California), 2004.

36. M. Omaña, D. Rossi, **C. Metra**, "Model for Transient Fault Susceptibility of Combinational Circuits", in *The Journal of Electronic Testing: Theory and Applications (JETTA),* Vol. 20, No. 5, pp. 495—503, October 2004, Kluwer Academic Publishers, Norwell, MA 02061 (USA), 2004.
37. M. Favalli**, C. Metra**, "TMR Voting in the Presence of Crosstalk Faults at the Voter Inputs", in *IEEE Transactions on Reliability,* Vol. 53, No. 3, pp. 342—348, September 2004, The Institute of Electrical and Electronics Engineers Inc., Piscataway, (NJ), 2004.
38. J. M. Cazeaux, D. Rossi and **C. Metra**, "Self-Checking Voter for High Speed TMR Systems", in *The Journal of Electronic Testing: Theory and Applications (JETTA),* Vol. 21, No. 4, August 2005, pp. 377—389, Springer, Springer Boston/Norwell (USA), 2005, ISSN: 0923-8174.
39. D. Rossi, A. K. Neiuwland, A. Kotoch and **C. Metra**, "Exploiting ECC Redundancy To Minimize Crosstalk Impact", in *IEEE Design & Test of Computers*, Vol. 22, N. 1, January-February, 2005, pp. 59—70, IEEE Computer Society Press, Los Alamitos (California), 2005.
40. D. Rossi, A. K. Nieuwland, A. Katoch, **C. Metra**, "New ECC for Crosstalk Impact Minimization", in *IEEE Design & Test of Computers*, July-August, 2005, pp.340—348, IEEE Computer Society Press, Los Alamitos (California), 2005.
41. M. Omaña, D. Rossi, **C. Metra,** "Low Cost and High Speed Embedded Two-Rail Code Checker", in *IEEE Transactions on Computers,* Vol. 54, Issue 2, February 2005, pp. 153—164, IEEE Computer Society Press, Los Alamitos (California), 2005.
42. J. M. Cazeaux, M. Omaña, and **C. Metra**, "Novel On-Chip Circuit for Jitter Testing in High-speed PLLs", in *IEEE Transactions on Instrumentations and Measurements,* Vol. 54, Issue 5, October 2005, pp. 1779—1788, The Institute of Electrical and Electronics Engineers Inc., Piscataway, (NJ), 2005.
43. **C. Metra,** D. Rossi, TM. Mak, "Won't On-Chip Clock Calibration Guarantee Performance Boost and Product Quality?", in *IEEE Transactions on Computers*, Vol. 56, No. 3, March, 2007, pp. 415-428, IEEE Computer Society Press, Los Alamitos (California), 2007.
44. D. Rossi, J. M. Cazeaux, **C. Metra,** F. Lombardi, "Modeling Crosstalk Effects in CNT Bus Architectures", in *IEEE Transactions on Nanotechnology*, Vol. 6, No. 2, March, 2007, pp. 133-145, The Institute of Electrical and Electronics Engineers Inc., Piscataway, (NJ), 2007.
45. D. Rossi, A.K. Nieuwland, **C. Metra**, "Simultaneous Switching Noise: The Relation Between Bus Layout and Coding", in ***IEEE Design & Test of Computers,*** Vol. 25, Issue 1, January-February 2008, pp.76-86, IEEE Computer Society Press, Los Alamitos (California), 2008.
46. M. Omaña, D. Rossi, **C. Metra,** "Latch Susceptibility to Transient Faults and New Hardening Approach", in *IEEE Transactions on Computers,* Vol. 56, Issue 9, September 2007, pp. 1255-1268, IEEE Computer Society Press, Los Alamitos (California), 2007.
47. Lombardi, **C. Metra**, "Guest Editors' Introduction: The State of the Art in Nanoscale CAD", in *IEEE Design & Test of Computers*, Vol. 24, July-August, pp. 302--303, 2007, IEEE Computer Society Press, Los Alamitos (California), 2007.
48. (Book Chapter) X. Ma, J. Huang, **C. Metra**, F. Lombardi, "Reversible and Testable Circuits for Molecular QCA Design", in *"Emerging Nanotechnologies",* ISSN 0929-1296, ISBN 978-0-387-74746-0, pp. 157-202, *Springer US*, 2007.
49. D. Rossi, M. Omaña, **C. Metra**, "Checker No-Harm Alarms and Design Approaches to Tolerate Them", in *The Journal of Electronic Testing: Theory and Applications (JETTA),* Vol. 24, Issue 1-3, June 2008, pp. 93-103, Springer, Springer Boston/Norwell (USA), 2008, ISSN: 0923-8174.
50. **(Updated Invited Paper) C. Metra,** "Majority Logic", in *Wiley Encyclopedia of Electrical and Electronics Engineering,* pp. 1-8, April 2007, Wiley & Sons., Inc., Publishers, New York (USA), 2007, accessible online: eeee@wiley.com.

51. D. Rossi, A.K. Nieuwland, V.E.S. van Dijk, R.P. Kleihorst, **C. Metra**, "Power Consumption of Fault-Tolerant Busses", in *IEEE Transactions on VLSI Systems*, Vol. 16, Issue 5, May 2008, pp. 542-553, The Institute of Electrical and Electronics Engineers Inc., Piscataway, (NJ), 2008.
52. X. Ma, J. Huang, **C. Metra**, F. Lombardi, "Reversible Gates and Testability of One Dimensional Arrays of Molecular QCA", *The Journal of Electronic Testing: Theory and Applications (JETTA)"*, Vol. 24, No. 1-3, pp. 297 – 311, June 2008, Springer, Springer Boston/Norwell (USA), 2008, ISSN: 0923-8174.
53. D. Rossi, J. M. Cazeaux, M. Omana, **C. Metra**, A. Chatterjee, "Accurate Linear Model for SET Critical Charge Estimation", *IEEE Transactions on VLSI Systems*, Vol. 17, No. 8, pp. 1161 – 1166, August 2009, The Institute of Electrical and Electronics Engineers Inc., Piscataway, (NJ), 2009.
54. M. Favalli, **C. Metra**, " Testing resistive open and bridging faults through pulse propagation", *IEEE Transactions on CAD*, Vol. 28, Issue 6, June 2009, pp. 915 – 925, The Institute of Electrical and Electronics Engineers Inc., Piscataway, (NJ).
55. M. Omaña, D. Rossi, **C. Metra,** "Latch High Performance Robust Latches", *IEEE Transactions on Computers*, Vol. 59, No. 11, pp. 1455 – 1465, November 2010, IEEE Computer Society Press, Los Alamitos (California), 2010.
56. **C. Metra**, M. Omaña**,** TM Mak, S. Tam, "Low-Cost Dynamic Compensation Scheme for Local Clocks of Next Generation High Performance Microprocessors", *IEEE Transactions on VLSI Systems*, Vol. 19, No. 12, pp. 2322 – 2325, December 2011, The Institute of Electrical and Electronics Engineers Inc., Piscataway, (NJ), 2011 (TVLSI-00007-2010)
57. **C. Metra**, M. Omaña**,** TM Mak, S. Tam, "New Design For Testability Approach for Clock Fault Testing", *IEEE Transactions on Computers,* Vol. 16, No. 61, April 2012, IEEE Computer Society Press, Los Alamitos (California), 2012 (TC-2009-11-0558)
58. M. Omaña**,** D. Rossi, N. Bosio, **C. Metra**, "Low Cost NBTI Degradation Detection & Masking Approaches", *IEEE Transactions on Computers,* Vol. 62, No. 3, pp. 496-509, March 2013, IEEE Computer Society Press, Los Alamitos (California), 2013
59. M. Omaña, D. Rossi, D. Giaffreda, R. Specchia, **C. Metra,** M. Marzencki, B. Kaminska, "Faults Affecting Energy Harvesting Circuits of Self-Powered Wireless Sensors and Their Possible Concurrent Detection", in *IEEE Transactions on VLSI Systems,* Vol. 21, Issue 12, December 2013, pp. 2286 – 2294, IEEE Computer Society Press, Los Alamitos (California), 2012
60. D. Rossi, M. Omaña, G. Garrammone, **C. Metra**, A. Jas, R, Galivanche, "Low Cost Concurrent Error Detection Strategy for the Control Logic of High Performance Microprocessors and Its Application to the Instruction Decoder", *The Journal of Electronic Testing: Theory and Applications (JETTA)"*, Vol. 29, No. 3, June 2013, pp. 401 – 413, Springer, Springer Boston/Norwell (USA), 2013
61. R. Vimalathithan, D. Rossi, M. Omaña, **C. Metra**, M.L.Valarmathi, "Polynomial Based Key Distribution Scheme for WPAN", *Malaysian Journal of Mathematical Sciences*, Special Edition of International Conference on Cryptology on Computer Security, Vol. 7(S), pp. 59-72, August 2013, ISSN: 1823-8343
62. D. Rossi, M. Omaña, J. M. Cazeaux, **C. Metra**, TM. Mak, "Clock Faults Induced Min and Max Delay Violations", in *Journal of Electronic Testing: Theory and Applications*, Volume 30, Issue 1, 2014, pp. 111-123, Springer, Springer Boston/Norwell (USA), 2014, Springer, Springer Boston/Norwell (USA), 2014
63. M. Omaña, D. Rossi, D. Giaffreda, **C. Metra,** TM Mak, A. Rahman, S. Tam, "Low-Cost On-Chip Clock Jitter Measurement Scheme", in *IEEE Transactions on Very Large Scale Integrated (VLSI) Systems*, Vol. 23, Issue 3, March 2015, pp. 435 – 443, IEEE Computer Society Press, Los Alamitos (California), 2015.

64. D. Rossi, **M. Omaña**, C. Metra, A. Paccagnella, "Impact of Bias Temperature Instability on Soft Error Susceptibility", in *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, Vol. 23 , Issue 4, April 2015, pp. 743 – 751, IEEE Computer Society Press, Los Alamitos (California), 2015.
65. D. Rossi, M. Omaña, D. Giaffreda, **C. Metra**, "Modeling and Detection of Hot-Spot in Shaded Photovoltaic Cells", *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, Vol. 23, Issue 6, June 2015, pp. 1031-1039
66. R. Vimalathithan, D. Rossi, M. Omaña, **C. Metra**, M. L. Valarmathi, "Cryptanalysis of Simplified-AES Encrypted Communication", *International Journal of Computer Science and Security (IJCSIS)*, Vol. 13 No. 10, October 2015, pp. 142 – 150.
67. M. Omaña, D. Rossi, E. Beniamino, **C. Metra**, C. Tirumurti, R. Galivanche, "Low-Cost and High-Reduction Approaches for Power Droop During Launch-On-Shift Scan-Based Logic BIST", *IEEE Trans. on Computers*, Vol. 65, Issue 8, August 2016, pp. 2484-2484,
68. M. Omaña, D. Rossi, T. Edara, **C. Metra**, "Impact of Aging Phenomena on Latches' Robustness", *IEEE Trans. on Nanotechnology*, Issue 2, March 2016, pp. 129-136,
69. M. Omaña, M. Padovani, K. Veliu, **C. Metra**, J. Alt, R. Galivanche, "New Approaches for Power Binning of High Performance Microprocessors", *IEEE Transactions on Computers*, Vol. 66, Issue 7, July 2017, pp. 1159-1171.
70. M. Omaña, D. Rossi, F. Fuzzi, **C. Metra**, C. Tirumurti, R. Galivanche, "Scalable Approach for Power Droop Reduction During Scan-Based Logic BIST", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 25, No. 1, January 2017, pp. 238 - 246.
71. **C. Metra,** "Message from the Editor-in-Chief", *IEEE Transactions on Emerging Topics in Computing*, Vol. 6, Issue 1, January-March 2018, pp. 3-4.
72. M. Omaña, T. Edara, **C. Metra**, "Low-Cost Strategy to Mitigate the Impact of Aging on Latches' Robustness", *IEEE Transactions on Emerging Topics in Computing*, Vol. 6, Issue 4, June 2018, pp. 488-497.
73. **C. Metra,** "Message from the Editor-in-Chief", *IEEE Transactions on Emerging Topics in Computing*, Vol. 7, Issue: 1, January-March 2019, pp. 3 – 4.
74. M. Omaña, A. Fiore, M. Mongitore, **C. Metra**, "Fault Tolerant Inverters for Reliable Photovoltaic Systems", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 27, Issue 1, January 2019, pp. 20-28.
75. M. Omaña, S. Goviandaraj, **C. Metra**, "Low-Cost Strategy for Bus Propagation Delay Reduction", *Journal of Electronic Testing: Theory and Applications (JETTA)*, Vol. 35, Number 2, April 2019, pp. 253 – 260.
76. **C. Metra**, "The 2019 IEEE Computer Society: Targeting Member Satisfaction and Technical Excellence", *Computer*, Vol. 52, Issue: 1, January 2019, pp. 4 – 6.
77. R. Aitken, **C. Metra,** "Special Section on Emerging Trends and Design Paradigms for Memory Systems and Storage", *IEEE Transactions on Emerging Topics in Computing*, Vol. 7, Issue: 3, July-September 2019, pp. 433 – 434.
78. **C. Metra**, "The 2019 IEEE Computer Society: Hit Target on Member Satisfaction and Technical Excellence", *Computer*, Vol. 52, Issue: 12, December 2019, pp. 4 – 11.
79. **C. Metra,** "Message from the Editor-in-Chief", *IEEE Transactions on Emerging Topics in Computing*, Vol. 8, Issue: 4, October-December 2020, pp. 885 – 886.
80. M. Omaña, S. Bardhan**, C. Metra**, "Reliability Risks Due to Faults Affecting Selectors of ReRAMs and Possible Solutions", *IEEE Transactions on Emerging Topics in Computing*, Vol. 10, No. 4, October-December 2022, pp. 2086-2091.
81. M. Omaña, M. Grossi, **C. Metra**, "Early Fault Detection in Inverters of Photovoltaic Systems", *Microelectronic Reliability*, Elsevier, Vol. 135, August 2022

82. M. Grossi, M. Bouras, M. Omaña, **C. Metra**, H. Berbia, "Low-Cost Strategy to Detect Faults Affecting Scrubbers in SRAM-Based FPGAs", *Microprocessors and Microsystems*, Elsevier, Vol. 89, 2022

Patents

83. **Co-inventor** of "*A Digital, Parallel, Clock Synchronizer"* (provisional US Patent OTT Ref #2505-3193).

84. **Co-inventor** (together with Kleihorst Richard, Nieuwland Andre, Van Dijk Victor, *Philips Research, Eindhoven, The Netherlands*) of "*Data Communication Using Fault Tolerant Error Correcting Codes and Having Reduced Ground Bounce"* (International Publication Number WO 2005/088465 A1, International Publication Date 22 September 2005).

Refereed International Conferences/Symposia/Workshops

85. **C. Metra**, M. Favalli, P. Olivo, B. Riccò, "CMOS Checkers with Testable Bridging and Transistor Stuck-on Faults", in *IEEE Proceedings of International Test Conference*, Baltimore (MD, USA), pp. 948–957, September 20-24, 1992, International Test Conference, 2000 L Street, NW, Washington D.C. 20036, 1992.
86. **C. Metra**, M. Favalli, P. Olivo, B. Riccò, "Testing of Resistive Bridging Faults in CMOS Flip-Flop", in *IEEE Proceedings of European Test Conference*, Rotterdam (The Netherlands), pp. 530–531, April 19-22, 1993, IEEE Computer Society Press, Los Alamitos (California), 1993.
87. **C. Metra**, M. Favalli, P. Olivo, B. Riccò, "Design Rules for CMOS Self Checking Circuits with Parametric Faults in the Functional Block", in *IEEE Proceedings of The IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems*, Venezia (Italy), pp. 271–278, October 27-29 October, 1993, IEEE Computer Society Press, Los Alamitos (California), 1993.
88. **C. Metra**, M. Favalli, P. Olivo, B. Riccò, "A Highly Testable 1-out-of-3 CMOS Checker", in *IEEE Proceedings of The IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems*, Venezia (Italy), pp. 279–286, October 27-29, 1993, IEEE Computer Society Press, Los Alamitos (California), 1993.
89. **C. Metra**, M. Favalli, B. Riccò, "CMOS Self Checking Circuits with Faulty Sequential Functional Blocks", in *IEEE Proceedings of The IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems*, Montreal (Canada), pp. 133–141, October 17-19, 1994, IEEE Computer Society Press, Los Alamitos (California), 1994.
90. **C. Metra**, M. Favalli, B. Riccò, "Highly Testable and Compact 1-out-of-n CMOS Checkers", in *IEEE Proceedings of The IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems*, Montreal (Canada), pp.142–150, October 17-19, 1994, IEEE Computer Society Press, Los Alamitos (California), 1994.
91. **C. Metra**, "MINIMAL POWER-DELAY PRODUCT CMOS BUFFER", in *Proceedings of Power And Timing Modeling, Optimization and Simulation'94 (PATMOS'94),* Barcellona (Spain), pp. 150–157, October 17-19, 1994, UPC, Barcellona (Spain), 1994.
92. **C. Metra**, M. Favalli, B. Riccò, "Highly Testable 1-out-of-n Dynamic CMOS Checker", in *Proceedings of 1st IEEE International On-Line Testing Workshop*, Nice (France), pp.248–252, July 4-6, 1995, CNRS, Grenoble (Francia), 1995.

93. **C. Metra**, M. Favalli, B. Riccò, "Glitch Power Dissipation Model", in *Proceedings of Power And Timing Modeling, Optimization and Simulation'95 (PATMOS'95),* Oldenburg (Germany), pp. 175–189, October 4-6, 1995, bis, Oldenburg (Germania), 1995.
94. M. Favalli, **C. Metra**, "The effect of glitches on CMOS Buffer Optimization", in *Proceedings of Power And Timing Modeling, Optimization and Simulation'95 (PATMOS'95),* Oldenburg (Germany), pp. 202–212, October 4-6, 1995, bis, Oldenburg (Germania), 1995.
95. **C. Metra**, M. Favalli, B. Riccò, "Novel Berger Code Checker", in *IEEE CS Proceedings of The IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems* 1995, Lafayette (Louisiana), pp.287–295, November 13-15, 1995, IEEE Computer Society Press, Los Alamitos (California), 1995.
96. **C. Metra,** M. Favalli, B. Riccò, "Embedded Two-Rail Checkers with On-Line Testing Ability", in *IEEE Proceedings of 14th IEEE VLSI Test Symposium*, Princeton (New Jersey), pp.145–150, April 28 – May 1, 1996, IEEE Computer Society Press, Los Alamitos (California), 1996.
97. **C. Metra,** M. Favalli, B. Riccò, "Embedded 1-out-of-3 Checkers with On-Line Testing Ability", in *Proceedings of 2nd IEEE International On-Line Testing Workshop,* Saint-Jean de-Luz, Biarritz (France), pp. 136–141, July 8-10, 1996, CNRS, Grenoble (France), 1996.
98. **C. Metra**, Jien-Chung Lo, "Compact and High Speed Berger Code Checker", in *Proceedings of 2nd IEEE International On-Line Testing Workshop*, Saint-Jean de-Luz, Biarritz (France), pp. 144–149, July 8-10, 1996, CNRS, Grenoble (Francia), 1996.
99. **C. Metra**, M. Favalli, B. Riccò, "Tree Checkers for Applications with Low Power-Delay Requirements", in *IEEE Proceedings of The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Boston (MA), pp. 213–220, November 6-8, 1996, IEEE Computer Society Press, Los Alamitos (California), 1996.
100. **C. Metra**, M. Favalli, B. Riccò, "Compact and Highly Testable Error Indicator for Self-Checking Circuits", in *IEEE Proceedings of The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Boston (MA), pp. 204–212, November 6-8, 1996, IEEE Computer Society Press, Los Alamitos (California), 1996.
101. M. Favalli, **C. Metra**, "Testing scheme for IC's clock", in *IEEE Proceedings of The European Design & Test Conference and Exhibition 1997*, Paris (France), pp. 445–449, March 17-20, 1997.
102. **C. Metra**, M. Favalli, B. Riccò, Highly Testable and Compact Single Output Comparator", in *IEEE Proceedings of 15th IEEE VLSI Test Symposium*, Monterey (California), pp. 210–215, April 27 – 30, 1997, IEEE Computer Society Press, Los Alamitos (California), 1997.
103. **C. Metra**, M. Favalli, B. Riccò, "Novel Single Output –out-of-3 Code Checker", in *Proceedings of 3rd IEEE International On-Line Testing Workshop*, Crete (Greece), pp. 228–232, July 7-9, 1997, Dept. of Computer Eng. & Informatics, Univ. of Patras, Greece, 1997.
104. **C. Metra**, M. Favalli, B. Riccò, "Self-Checking Detector for Simultaneous On-Line Test of Clock Signals", in *Proceedings of 3rd EEE International On-Line Testing Workshop*, Crete (Greece), pp. 79–83, July 7-9, 1997, Dept. of Computer Eng. & Informatics, Univ. of Patras, Greece, 1997.
105. M. Favalli, **C. Metra**, "Leakage power reduction for reactive computation", in *Proceedings of Power And Timing Modeling, Optimization and Simulation'97 (PATMOS'97),* Louvain-la-Neuve (Belgium), pp. 57–66, September 8-10, 1997, Presses Universitaires de Louvain-la-Neuve, Luovain (Belgium), 1997.
106. **C. Metra**, M. Favalli, B. Riccò, "On-Line Testing Scheme for Clocks' Faults", in *IEEE Proceedings of International Test Conference*, Washington, D.C. (USA), pp. 587–596, November 1-6, 1997, International Test Conference, 2000 L Street, NW, Washington D.C. 20036, 1997.
107. **C. Metra**, M. Favalli, B. Riccò, "Compact and Low Power Self-Checking Voting Scheme", in *IEEE Proceedings of The International Symposium on Defect and Fault-Tolerance in VLSI*

Systems, Paris (France), pp. 137–145, October 20-22, 1997, IEEE Computer Society Press, Los Alamitos (California), 1997.

108. M. Favalli, **C. Metra**, "Low-level Error Recovery Mechanism for Self-Checking Sequential Circuits", in *IEEE Proceedings of The International Symposium on Defect and Fault-Tolerance in VLSI Systems*, Paris (France), pp. 234–242, October 20-22, 1997, EEE Computer Society Press, Los Alamitos (California), 1997.
109. Y-Y. Guo, J-C. Lo, **Cecilia Metra**, "Fast and Area-Time Efficient Berger Code Checkers", in *IEEE Proceedings of The International Symposium on Defect and Fault-Tolerance in VLSI Systems*, Paris (France), pp.110–118, October 20-22, 1997, IEEE Computer Society Press, Los Alamitos (California), 1997.
110. **C. Metra**, M. Favalli, B. Riccò, "Highly Testable and Compact 1-out-of-n Code Checker with Single Output", in *IEEE Proceedings of Design, Automation and Test in Europe*, Paris (France), pp. 981–982, February 23-26, 1998, IEEE Computer Society Press, Los Alamitos (California), 1998.
111. **C. Metra**, Giovanni Mojoli, Sandro Pastore, Davide Salvi, Giacomo Sechi, "Novel Technique for Testing FPGAs", in *IEEE Proceedings of Design, Automation and Test in Europe*, Paris (France), pp. 89–94, February 23-26, 1998, IEEE Computer Society Press, Los Alamitos (California), 1998.
112. **(Invited) C. Metra**, "Concurrent Testing Techniques for Clock's Faults", in *Lecture Notes of the Intel Research Symposium VLSI Test*, Santa Clara (CA), pp. 1–47, April 24, 1998, Intel Corporation, Santa Clara (CA).
113. **C. Metra,** M. Favalli, B. Riccò, "Novel Implementation for Highly Testable Parity Code Checkers", in *Compendium of Papers of 4th IEEE International On-Line Testing Workshop*, Capri (Italy), pp. 167–171, July 6-8, 1998, Politecnico di Torino, Dip. Di Automatica e Informatica, Torino (Italy), 1998.
114. **C. Metra**, J-C. Lo, "General Design Method for VLSI High Speed Berger Code Checkers", in *Compendium of Papers of 4th IEEE International On-Line Testing Workshop*, Capri (Italy), pp.177–181, July 6-8, 1998, Politecnico di Torino, Dip. Di Automatica e Informatica, Torino (Italy), 1998.
115. **C. Metra**, M. Favalli, B. Riccò, "On-Line Detection of Logic Errors due to Crosstalk, Delay and Transient Faults", in *IEEE Proceedings of International Test Conference*, Washington, D. C. (USA), pp. 524–533, October 18-23, 1998, International Test Conference, 2000 L Street, NW, Washington D.C. 20036, 1998.
116. **C. Metra**, M. Favalli, B. Riccò, "Signal Coding Technique and CMOS Gates for Strongly Fault-Secure Combinational Functional Blocks", in *IEEE Proceedings of The IEEE Symposium on Defect and Fault Tolerance in VLSI Systems*, Austin (Texas), pp. 174–182, November 2-4, 1998, IEEE Computer Society Press, Los Alamitos (California), 1998.
117. S. D'Angelo, **C. Metra**, S. Pastore, A. Pogutz, G. Sechi, "Fault-Tolerant Voting Mechanism and Recovery Scheme for TMR FPGA-based Systems", in *IEEE Proceedings of The IEEE Symposium on Defect and Fault Tolerance in VLSI Systems*, Austin (Texas), pp. 233–240, November 2-4, 1998, IEEE Computer Society Press, Los Alamitos (California), 1998.
118. M. Favalli, **C. Metra**, "On the design of self-checking functional units based on Shannon circuits", in *IEEE Proceedings of Design Automation and Test in Europe Conference*, Monaco (Germany), pp. 368–375, March 9-12, 1999, IEEE Computer Society Press, Los Alamitos (California), 1999.
119. **C. Metra**, F. Giovanelli, M. Soma, B. Riccò, "Self-Checking Scheme for Very Fast Clock's Skew Correction", in *IEEE Proceedings of International Test Conference*, Atlantic City, NJ (USA), pp.~652–661, September 28-30, 1999, International Test Conference, 2000 L Street, NW, Washington D.C. 20036, 1999.

120. **C. Metra**, R. Degiampietro, M. Favalli, B. Riccò, "Concurrent Detection and Diagnosis Scheme for Transient, Delay and Crosstalk Faults", in *IEEE Proceedings of 5th IEEE International On-Line Testing Workshop,* Rhodes, Greece, pp. 66–70, July 5-7, 1999, Dept. of Computer Eng. & Informatics, Univ. of Patras, Greece, 1999.
121. **C. Metra**, S. D'Angelo, G. Sechi, "Low Performance Degradation Transient Fault Recovery for TMR Systems", in *IEEE Proceedings of 5th IEEE International On-Line Testing Workshop,* Rhodes, Greece, pp. 44–48, July 5-7, 1999, Dept. of Computer Eng. & Informatics, Univ. of Patras, Greece, 1999.
122. S. D'Angelo, **C. Metra**, G. Sechi, "Transient and Permanent Fault Diagnosis for FPGA-Based TMR Systems", in *IEEE Proceedings of The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems,* November 1-3, 1999, Albuquerque (New Mexico), IEEE Computer Society Press, Los Alamitos (California), 1999.
123. **C. Metra,** M. Favalli, B. Riccò, "On-Line Testing and Diagnosis of Bus Lines with respect to Intermediate Voltage Values", in *IEEE Proceedings of Design, Automation and Test in Europe (DATE) Conference,* Paris (France), pp.763, March 27-30, 2000, IEEE Computer Society Press, Los Alamitos (California), 2000.
124. **C. Metra**, M. Favalli, B. Riccò, "On-Line Testing and Diagnosis Scheme for Intermediate Voltage Values Affecting Bus Lines", in *IEEE Proceedings of IEEE International Defect Based Testing Workshop,* Montreal (Canada), pp. 76–81, April 29, 2000, IEEE Computer Society Press, Los Alamitos (California), 2000.
125. M. Alderighi, S. D'Angelo, **C. Metra**, G. Sechi, "Achieving Fault Tolerance by Shifted and Rotated Operands in TMR non-Diverse ALUs", in *IEEE Proceedings of The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems,* Mt. Fuji (Japan), pp. 155–163, October 25-27, 2000, IEEE Computer Society Press, Los Alamitos (California), 2000.
126. M. Favalli, **C. Metra**, "Optimization of error detecting codes for the detection of crosstalk originated errors", in *IEEE Proceedings of Design, Automation and Test in Europe (DATE) Conference,* Munich (Germany), pp. 290–296, March 13-16, 2001, IEEE Computer Society Press, Los Alamitos (California), 2001.
127. M. Alderighi, S. D'Angelo, **C. Metra**, G. Sechi, "Novel Fault-Tolerant Adder Design for FPGA – Based Systems", in *IEEE Proceedings of 7th IEEE International On-Line Testing Workshop,* Giardini Naxos-Taormina (Italy), pp. 54–58, July 9-11, 2001, IEEE Computer Society Press, Los Alamitos (California), 2001.
128. M. Favalli, **C. Metra**, "Single Output Distributed Two-Rail Checker with Diagnosing Capabilities for Bus Based Self-Checking Architectures*",* in *IEEE Proceedings of 7th IEEE International On-Line Testing Workshop,* Giardini Naxos-Taormina (Italy), pp. 100–105, July 9-11, 2001, IEEE Computer Society Press, Los Alamitos (California), 2001.
129. **C. Metra**, A. Pagano, B. Riccò, "On-Line Testing of Transient and Crosstalk Faults Affecting Interconnections of FPGA-Implemented Systems", in *IEEE Proceedings of International Test Conference (ITC),* Baltimore (MD), pp. 939–947, October 30 – November 1, 2001, International Test Conference, 2000 L Street, NW, Washington D.C. 20036, 2001.
130. **C. Metra**, S. Di Francescantonio, T. M. Mak, B. Riccò, "Evaluation of Clock Distribution Networks' Most Likely Faults and Produced Effects", in *IEEE Proceedings of The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, pp. 357–365, October 24-26, 2001, San Francisco (CA, USA), IEEE Computer Society Press, Los Alamitos (California), 2001.
131. M. Favalli, **C. Metra**, "Problems due to open faults in the interconnections of self-checking data-paths", in *IEEE Proceedings of Design, Automation and Test in Europe (DATE) Conference,* Paris

(France), March 4-8, pp. 612–617, 2002, IEEE Computer Society Press, Los Alamitos (California), 2002.
132. **C. Metra**, L. Schiano, M. Favalli, B. Riccò, "Self-Checking Scheme for the On-Line Testing of Power Supply Noise", in *IEEE Proceedings of Design, Automation and Test in Europe (DATE) Conference,* Paris (France), pp. 832–836, March 4-8, 2002, IEEE Computer Society Press, Los Alamitos (California), 2002.
133. D. Rossi, V.E.S. van Dijk, R.P. Kleihorst, A.H. Nieuwland and **C. Metra**, "Coding Scheme for Low Energy Consumption Fault-Tolerant Bus", in *IEEE Proceedings 8th IEEE International On-Line Testing Workshop,* Isle of Bendor (France), pp. 8–12, July 8-10, 2002, IEEE Computer Society Press, Los Alamitos (California), 2002.
134. L. Schiano, **C. Metra** and D. Marino, "Design and Implementation of a Self-Checking Scheme for Railway Trackside Systems", in *IEEE Proceedings 8th IEEE International On-Line Testing Workshop*, Isle of Bendor (France), pp. 243–247, July 8-10, 2002, IEEE Computer Society Press, Los Alamitos (California), 2002.
135. D. Rossi, **C. Metra** and B. Riccò, "Fast and Compact Error Correcting Scheme for Reliable Multilevel Flash Memories", in *IEEE Proceedings IEEE International Workshop on Memory Technology, Design and Testing*, Isle of Bendor (France), pp. 27–31, July 10-12, 2002, IEEE Computer Society Press, Los Alamitos (California), 2002.
136. **C. Metra**, S. Di Francescantonio, T. M. Mak, "Clock Faults' Impact on Manufacturing Testing and Their Possible Detection Through On-line Testing", in *IEEE Proceedings of International Test Conference (ITC),* Baltimore (MD), October 8-10, 2002, pp. 100-109, International Test Conference, 2025 M Street, N.W., Suite 800, Washington D.C., 20036, 2002.
137. **C. Metra**, S. Di Francescantonio, G. Marrale, "On-Line Testing of Transient faults Affecting Functional Blocks of FCMOS, Domino and FPGA-Implemented Self-Checking Circuits", in *IEEE Proceedings of The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, November 6-8, 2002, Vancouver (Canada), pp. 207-215, IEEE Computer Society Press, Los Alamitos (California), 2002.
138. M. Omaña, D. Rossi and **C. Metra**, "High Speed and Highly Testable Parallel Two- Rail Code Checker", in *IEEE Proceedings of Design, Automation and Test in Europe (DATE) Conference,* Munich (Germany), pp. 608–613, March 4-7, 2003, IEEE Computer Society Press, Los Alamitos (California), 2003.
139. D. Rossi, V.E.S. van Dijk, R.P. Kleihorst, A.H. Nieuwland and **C. Metra**, "Power Consumption of Fault Tolerant Codes: the Active Elements", in *IEEE Proceedings 9th IEEE International On-Line Testing Symposium",* Kos (Greece), July 7 – 9, 2003, pp. 61-67, IEEE Computer Society Press, Los Alamitos (California), 2003.
140. L. Di Silvio, D. Rossi and **C. Metra**, "Crosstalk effect minimization for encoded bus", in *IEEE Proceedings 9th IEEE International On-Line Testing Symposium*, Kos (Greece), July 7 – 9, 2003, pp. 214-218, IEEE Computer Society Press, Los Alamitos (California), 2003.
141. M. Omaña, G. Papasso, D. Rossi and **C. Metra**, "A Model for Transient Fault Propagation in Combinatorial Logic", in *IEEE Proceedings 9th IEEE International On-Line Testing Symposium*, Kos (Greece), July 7 – 9, 2003, pp. 111-115, IEEE Computer Society Press, Los Alamitos (California), 2003.
142. M. Omaña, D. Rossi, **C. Metra**, "Novel Transient Fault Hardened Static Latch", in *IEEE Proceedings of International Test Conference (ITC),* Baltimore (MD), September 30 – October 2, 2003, pp. 886-892, International Test Conference, 2025 M Street, N.W., Suite 800, Washington D.C., 20036, 2003.
143. **C. Metra,** S. Di Francescantonio, M. Omana, "Automatic Modification of Sequential Circuits for Self-Checking Implementation", in *IEEE Proceedings of The International Symposium on*

Defect and Fault Tolerance in VLSI Systems, Boston (MA), November 2003, pp. 417-424, IEEE Computer Society Press, Los Alamitos (California), 2003.

144. D. Rossi, S. Cavallotti, **C. Metra,** "Error Correcting Codes for Crosstalk Effect Minimization", in *IEEE Proceedings of The International Symposium on Defect and Fault Tolerance in VLSI Systems*, Boston (MA), November 2003, pp. 257-264, IEEE Computer Society Press, Los Alamitos (California), 2003.
145. **C. Metra,** TM Mak, D. Rossi, "Clock Calibration Faults and their Impact on Quality of High Performance Microprocessors", in *IEEE Proceedings of The International Symposium on Defect and Fault Tolerance in VLSI Systems*, Boston (MA), November 2003, pp.63-70, IEEE Computer Society Press, Los Alamitos (California), 2003.
146. **C. Metra,** TM Mak, M. Omaña, "Are Our Design For Testability Features Fault Secure ?", in *IEEE Proceedings of Design, Automation and Test in Europe (DATE) Conference*, Paris (France), pp. 714—715, February 16-20, 2004, IEEE Computer Society Press, Los Alamitos (California), 2004.
147. J. M. Cazeaux, M. Omaña, **and C. Metra**, "Low-Area and Fast On-Chip Circuit for Jitter Measurement in Phase-Locked Loop", in *IEEE Proceedings 10th IEEE International On-Line Testing Symposium*, Madeira (Portugal), July 12 – 14, 2004, pp. 17-22, IEEE Computer Society Press, Los Alamitos (California), 2004.
148. J. M. Cazeaux, D. Rossi and **C. Metra**, "New High Speed CMOS Self-Checking Voter", in *IEEE Proceedings 10th IEEE International On-Line Testing Symposium*, Madeira (Portugal), July 12 – 14, 2004, pp. 58-63, IEEE Computer Society Press, Los Alamitos (California), 2004.
149. **C. Metra,** TM Mak, M. Omaña, "Fault Secureness Need for Next Generation High Performance Microprocessor Design for Testability Structures", in *Proceedings of 2004 ACM International Conference on Computing Frontiers*, Ischia (Italy), pp. 444—450, April 14-16, 2004, ACM ISBN: 1-58113-741-9.
150. **C. Metra**, A. Ferrari, M. Omaña and A. Pagni, "Hardware Reconfiguration Scheme for High Availability Systems", in *IEEE Proceedings 10th IEEE International On-Line Testing Symposium*, Madeira (Portugal), July 12 – 14, 2004, pp. 161-166, IEEE Computer Society Press, Los Alamitos (California), 2004.
151. D. Rossi, A. Muccio, A. K. Neiuwland, A. Kotoch and **C. Metra**, "Impact of ECCs on Simultaneously Switching Outputs Noise for On-Chip Busses of High Reliability Systems", in *IEEE Proceedings 10th IEEE International On-Line Testing Symposium*, Madeira (Portugal), July 12 – 14, 2004, pp. 135-140 IEEE Computer Society Press, Los Alamitos (California), 2004.
152. **C. Metra,** TM Mak, M. Omaña, "Should We Make Our Design for Testability Schemes Fault Secure ?", in *IEEE Proceedings of The IEEE European Test Symposium*, Aiaccio (Corsica), pp. 67—72, May, 2004.
153. **C. Metra,** M. Omaña, TM Mak, "Risks Associated with Faults within Test Pattern Compactors and Their Implications on Testing", in *IEEE Proceedings of International Test Conference (ITC)*, Charlotte (NC), pp. 1223 – 1231, October 26- October 28, 2004, International Test Conference, 2025 M Street, N.W., Suite 800, Washington D.C., 20036, 2004.
154. M. Omaña, D. Rossi, **C. Metra,** "Fast and Low Cost Deskew Buffer", in *IEEE Proceedings of The International Symposium on Defect and Fault Tolerance in VLSI Systems*, Cannes (France), October 11-13, 2004, pp. 202 – 210, IEEE Computer Society Press, Los Alamitos (California), 2004.
155. M. Omaña, D. Rossi, **C. Metra,** "Low Cost Scheme for On-Line Clock Skew Compensation", in *IEEE Proceedings of 23rd IEEE VLSI Test Symposium*, Palm Springs (California), May 1-5, 2005, pp. 90—95, IEEE Computer Society Press, Los Alamitos (California), 2005.

156. J. M. Cazeaux, D. Rossi, M. Omaña, **C. Metra**, and A. Chatterjee, "On Transistor Level Gate Sizing for Increased Robustness to Transient Faults", in *IEEE Proceedings 11th IEEE International On-Line Testing Symposium*, Saint Raphael (France), July 6-8, 2005, pp. 23—28, IEEE Computer Society Press, Los Alamitos (California), 2005.
157. M. Omaña, O. Losco, **C. Metra** and A. Pagni, "On the Selection of Unidirectional Error Detecting Codes for Self-Checking Circuits' Area Overhead and Performance Optimization", in *IEEE Proceedings 11th IEEE International On-Line Testing Symposium*, Saint Raphael (France), July 6-8, 2005, pp. 163—168, IEEE Computer Society Press, Los Alamitos (California), 2005.
158. A. K. Nieuwland, A. Katoch, D. Rossi and **C. Metra**, "Coding Techniques for Low Switching Noise in Fault Tolerant Busses", in *IEEE Proceedings 11th IEEE International On-Line Testing Symposium*, Saint Raphael (France), July 6-8, 2005, pp. 183—189, IEEE Computer Society Press, Los Alamitos (California), 2005.
159. Y. S. Dhillon, A. U. Diril, A. Chatterjee, and **C. Metra**, "Output Load and Logic Co-Optimization for Design of Soft-Error Resistant Nanometer CMOS Circuits", in *IEEE Proceedings 11th IEEE International On-Line Testing Symposium*, Saint Raphael (France), July 6-8, 2005, pp. 35—40, IEEE Computer Society Press, Los Alamitos (California), 2005.
160. **C. Metra,** M. Omaña, D. Rossi, JM. Cazeaux, TM Mak, "The Other Side of the Timing Equation: a Result of Clock Faults", in *IEEE Proceedings of The International Symposium on Defect and Fault Tolerance in VLSI Systems*, Monterey (California), October 3-5, 2005, pp. 169—177, IEEE Computer Society Press, Los Alamitos (California), 2005.
161. D. Rossi, M. Omaña, F. Toma, **C. Metra,**, "Multiple Transient Faults in Logic: an Issue for Next Generation Ics ?", in *IEEE Proceedings of The International Symposium on Defect and Fault Tolerance in VLSI Systems*, Monterey (California), October 3-5, 2005, pp. 352—360, IEEE Computer Society Press, Los Alamitos (California), 2005.
162. D. Rossi, C. Steiner, **C. Metra,** "Analysis of the Impact of Bus Implemented EDCs on On-Chip SSN", in *IEEE Proceedings of the Design, Automation and Test in Europe (DATE 2006),* Munich (Germany), March 6-10, 2006, pp. 59—64, IEEE Computer Society Press, Los Alamitos (California), 2006.
163. M. Omaña, J. M. Cazeaux, D. Rossi, **C. Metra,** "Low-Cost and Highly Reliable Detector for Transient and Crosstalk Faults Affecting FPGA Interconnects", in *IEEE Proceedings of IEEE Design, Automation and Test in Europe (DATE 2006),* Munich (Germany) March 6 – 10, 2006, pp. 170—175, IEEE Computer Society Press, Los Alamitos (California), 2006.
164. **C. Metra**, D. Rossi, M. Omaña, J.M. Cazeaux, TM Mak, "Can Clock Faults Be Detected Through Functional Test ?", *Proc. of the 9th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems (DDECS'06),* Prague (Czech Republic), April 18 – 21, 2006, pp. 168—173, ISBN: 1-4244-0184-4.
165. D. Rossi, M. Omaña, **C. Metra,** A. Pagni, "Checker No-Harm Alarm Robustness", in *IEEE Proceedings of the IEEE International On-Line Testing Symposium*, Como (Italy), July 10-12, 2006, pp.275—280, IEEE Computer Society Press, Los Alamitos (California), 2006.
166. **C. Metra,** M. Omaña, D. Rossi, J. M. Cazeaux, TM Mak, "Path (Min) Delay Faults and Their Impact on Self-Checking Circuits' Operation", in *IEEE Proceedings of the IEEE International On-Line Testing Symposium*, Como (Italy), July 10-12, 2006, pp.17—22, IEEE Computer Society Press, Los Alamitos (California), 2006.
167. D. Rossi, J. M. Cazeaux, **C. Metra,** F. Lombardi, "A Novel Dual-Walled CNT Bus Architecture with Reduced Cross-Coupling Features", in *IEEE Proceedings of the IEEE Conference on Nanotechnology*, Cincinnati (Ohio, USA), July 16-20, 2006, IEEE Catalog number 06TH8861C, ISBN 1-4244-0078-3.

168. X. Ma, J. Huang, **C. Metra**, F. Lombardi, "Testing Reversible 1D Arrays of Molecular QCA", in *IEEE Proceedings of The International Symposium on Defect and Fault Tolerance in VLSI Systems,* Washington DC (USA), October 4—6, 2006, IEEE Computer Society Press, Los Alamitos (California), 2006.
169. M. Favalli, **C. Metra**, "Pulse propagation for the detection of small delay defects", in *IEEE Proceedings of the Design, Automation and Test in Europe (DATE 2007),* Nice (France), April 16-20, 2007, IEEE Computer Society Press, Los Alamitos (California), 2007.
170. D. Rossi, P. Angelini, **C. Metra**, "Configurable Error Control Scheme for NoC Signal Integrity", in *IEEE Proceedings of the IEEE International On-Line Testing Symposium,* Crete (Greece), July 9-11, 2007 pp. 1-6, IEEE Computer Society Press, Los Alamitos (California), 2007.
171. **C. Metra**, M. Omaña, TM. Mak, S. Tam, "Novel Approach to Clock Fault Testing for High Performance Microprocessors", in *IEEE Proceedings VLSI Test Symposium 2007,* May 6-9, Berkeley, CA, 2007, pp. 441—446, IEEE Computer Society Press, Los Alamitos (California), 2007.
172. X. Ma, J. Huang, **C. Metra**, F. Lombardi, "Testing Reversible One-Dimensional QCA Arrays for Multiple Faults", in *IEEE Proceedings of The International Symposium on Defect and Fault Tolerance in VLSI Systems 2007,* Rome (Italy), September 26-28, 2007, pp. 469-477, IEEE Computer Society Press, Los Alamitos (California), 2007.
173. **C. Metra**, M. Omaña, TM. Mak, S. Tam, "Novel Compensation Scheme for Local Clocks of High Performance Microprocessors", in *IEEE Proceedings of the IEEE International Test Conference 2007,* Santa Clara (California), October 21-26, 2007, pp. 1-9, International Test Conference, 2025 M Street, N.W., Suite 800, Washington D.C., 20036, 2007.
174. D. Rossi, P. Angelini, **C. Metra**, G. Campardo, GP Vanelli, "Risks for Signal Integrity in System in Package and Possible Remedies", in *IEEE Proceedings* of the *IEEE European Test Symposium 2008*, Lake Maggiore (Italy), May 25-29, pp. 165—170, 2008, IEEE Computer Society Press, Los Alamitos (California), 2008.
175. **C. Metra**, D. Rossi, M. Omaña, A. Jas, R. Galivanche, "Function-Inherent Code Checking: A New Low Cost On-Line Testing Approach For High Performance Microprocessor Control Logic", in *IEEE Proceedings* of the *IEEE European Test Symposium 2008*, Lake Maggiore (Italy), May 25-29, pp. 171—176, 2008, IEEE Computer Society Press, Los Alamitos (California), 2008.
176. **C. Metra**, M. Omaña, TM Mak, A. Rahman, S. Tam, "Novel On-Chip Clock Jitter Measurement Scheme For High Performance Microprocessors", *IEEE Proceedings of the 23th IEEE Int. Symposium on Defect and Fault Tolerance in VLSI Systems* (DFT'08), Cambridge (MA), October 1-3, pp. 465-473, 2008, IEEE Computer Society Press, Los Alamitos (California), 2008.
177. X. Ma, J. Huang, F. Chiminazzo, D. Rossi, **C. Metra**, F. Lombardi, "Resistive Crossbar Switching Networks to Implement Inherently Fault Tolerant Nano LUTs", *IEEE Proceedings of the 1st IEEE International Workshop on Design and Test of Nano Devices, Circuits and Systems* (NDCS'08), Cambridge (MA), September 29-30, 2008, pp. 21 – 24, 2008,, IEEE Computer Society Press, Los Alamitos (California), 2008.
178. **C. Metra**, D. Rossi, M. Omaña, A. Jas, R. Galivanche, "Low Cost On-Line Testing of the Scheduler of High Performance Microprocessors", *Proceedings* of the *IEEE European Test Symposium 2009*, Sevilla (Spain), May 25-29, 2009.
179. **C. Metra**, "Trading Off Dependability and Cost for Nanoscale High Performance Microprocessors: The Clock Distribution Problem", *Proceedings* of the *IEEE Workshop on Dependable and Secure Nanocomputing 2009 (WDSN09),* Estoril (Portugal), June 29, 2009, pp. D4-D5, 2009, IEEE Catalog Number: CFP09048-CDR, ISBN: 978-1-4244-4421-2, Library of Congress: 2009902897

180. **(Best Paper Award)** M. Omaña, D. Rossi, **C. Metra**, "Novel High Speed Robust Latch", *IEEE Proceedings of the 23th IEEE Int. Symposium on Defect and Fault Tolerance in VLSI Systems* (DFT'09), Chicago (IL), October 7-9, pp. 65-73, 2009, IEEE Computer Society Press, Los Alamitos (California), 2009.
181. M. Omaña, M. Marzencki, R. Specchia, **C. Metra**, B. Kaminska, "Concurrent Detection of Faults Affecting Energy Harvesting Circuits of Self-Powered Wearable Sensors", *IEEE Proceedings of the 23th IEEE Int. Symposium on Defect and Fault Tolerance in VLSI Systems* (DFT'09), Chicago (IL), October 7-9, pp.127-135, 2009, IEEE Computer Society Press, Los Alamitos (California), 2009.
182. M. Omaña, D. Rossi, N. Bosio, **C. Metra**, "Novel Low-Cost Aging Sensor", in *ACM Proceedings of the International Conference on Computing Frontiers*, Bertinoro (Italy), May 17-19, 2010.
183. D. Rossi, M. Omaña, G Berghella, **C. Metra**, A. Jas, T. Chandra, R. Galivanche, "Low Cost and Low Intrusive Approach to Test On-Line the Scheduler of High Performance Microprocessors", in *ACM Proceedings of the International Conference on Computing Frontiers*, Bertinoro (Italy), May 17-19, 2010.
184. M. Omaña, D. Rossi, N. Bosio, **C. Metra,** "Self-Checking Monitor for NBTI Due Degradation", in *Proc. of IEEE International Mixed-Signals, Sensors, and Systems Test Workshop*, June 7-9, 2010, Montpellier, France, 2010.
185. D. Rossi, M. Omaña, D. Giaffreda, **C. Metra,** "Secure Communication Protocol for Wireless Sensor Networks", in IEEE Proc. of the *8th IEEE East-West Design & Test Symposium (EWDTS)*, September 17-20, 2010, IEEE Computer Society Press, Los Alamitos (California), 2010.
186. M. Omaña, D. Giaffreda, **C. Metra**, TM Mak, S. Tam, A. Rahman, "On-Die Ring Oscillator Based Measurement Scheme for Process Parameter Variations and Clock Jitter", *IEEE Proceedings of the 24th IEEE Int. Symposium on Defect and Fault Tolerance in VLSI Systems* (DFT'10), Kyoto (Japan), October 6-8, 2010, IEEE Computer Society Press, Los Alamitos (California), 2010.
187. D. Rossi, M. Omaña, **C. Metra**, "Transient Fault and Soft Error on-Die Monitor", *IEEE Proceedings of the 24th IEEE Int. Symposium on Defect and Fault Tolerance in VLSI Systems* (DFT'10), Kyoto (Japan), October 6-8, 2010, IEEE Computer Society Press, Los Alamitos (California), 2010.
188. D. Rossi, N. Timoncini, M. Spica, **C. Metra,** "Error Correcting Code Analysis for Memory High Reliability and Performance", in *IEEE Proc. of the Design, Automation and Test in Europe (DATE 2011)*, Grenoble (France), March 14-18, 2011, IEEE Computer Society Press, Los Alamitos (California), 2011.
189. D. Rossi, M. Omaña, **C. Metra**, A. Paccagnella, "Impact of Aging Phenomena on Soft Error Susceptibility", *IEEE Proceedings of the IEEE Int. Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems* (DFT'11), Vancouver (Canada), October 3-5, 2011, pp.18-24, IEEE Computer Society Press, Los Alamitos (California), 2011.
190. D. Giaffreda, M. Omaña, D. Rossi, **C. Metra**, "Model for Thermal Behavior of Shaded Photovoltaic Cells Under Hot-Spot Condition", *IEEE Proceedings of the IEEE Int. Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems* (DFT'11), Vancouver (Canada), October 3-5, 2011, pp. 252-258, IEEE Computer Society Press, Los Alamitos (California), 2011.
191. M. Omaña, D. Rossi, G. Collepalumbo, **C. Metra,** F. Lombardi, "Faults Affecting the Control Blocks of PV Arrays and Techniques for Their Concurrent Detection", in *IEEE Proceedings of the 25th IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems* (DFT'12), Austin (Texas, USA), October 3-5, 2012, pp. 199-204, IEEE Computer Society Press, Los Alamitos (California), 2012.

192. R. Vimalathithan, D. Rossi, M. Omaña, **C. Metra,** M. L. Valarmathi, "Polynomial Based Key Distribution Scheme for WPAN", in *Proceedings of 3rd International Conference on Cryptology and Computer Security 2012*, June 4-6 2012, Langkawi, Malaysia, 2012.
193. C. Bolchini, A. Miele, C. Sandionigi, M. Ottavi, S. Pontarelli, A. Salsano, **C. Metra,** M. Omaña, D. Rossi, M. Sonza Reorda, L. Sterpone, M. Violante, S. Gerardin, M. Bagatin, A. Paccagnella, "High-reliability Fault Tolerant Digital Systems in Nanometric Technologies: Characterization and Design Methodologies" in *IEEE Proceedings of the 25th IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems* (DFT'12), Austin (Texas, USA), October 3-5, 2012, pp. 121-125, IEEE Computer Society Press, Los Alamitos (California), 2012.
194. M. Omaña, F. Fuzzi, D. Rossi, **C. Metra**, C. Tirumurti, R. Galivanche, "Novel Approach to Reduce Power Droop During Scan-Based Logic BIST", in *IEEE Proceedings* of the *IEEE European Test Symposium 2013*, Avignon (France), May 27-31, 2013, IEEE Computer Society Press, Los Alamitos (California), 2013.
195. M. Omaña, D. Rossi, E. Beniamino, **C. Metra**, C. Tirumurti, and R. Galivanche, "Power Droop Reduction During Launch-On-Shift Scan-Based Logic BIST" in *IEEE Proceedings of IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems*, Amsterdam, October 1-3, 2014, pp. 21-26, IEEE Computer Society Press, Los Alamitos (California), 2014.
196. M. Omaña, L. A. Adanaque, **C. Metra,** D. Rossi, "On Aging of Latches' Robustness", in *Proc. of Manufacturable and Dependable Multicore Architectures at Nanoscale (MEDIAN) Workshop*, 2015.
197. M. A. Koche, A. Dalirsni, A. Bernabei, M. Omaña, **C. Metra,** H.-J. Wunderlich, "Intermittent and Transient Fault Diagnosis on Sparse Code Signatures", in *IEEE Proc. of Int'l. Asian Test Sympsium*, Mumbay (India), 22-25 November, 2015, pp. 157 – 162.
198. M. Omaña, A. Fiore, **C. Metra**, "Inverters' Self-Checking Monitors for Reliable Photovoltaic Systems", in *IEEE Proceedings of IEEE Design, Automation and Test in Europe (DATE 2016)*, Dresden (Germany), 14 – 18 March, 2016, pp. 672 – 677.
199. **C. Metra**, "Test and Reliability Challenges for High Performance, Nanotechnology Circuits and Systems", in *IEEE Proceedings of IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS)*, Košice (Slovakia), April 20-22, 2016, pp. 1-2
200. M. Grossi, M. Omaña, D. Rossi, **C. Metra**, "Novel BTI Robust Ring-Oscillator-Based Physically Unclonable Function", in *IEEE Proceedings of the 28th IEEE International On-Line Testing Symposium*, Torino (Italy), September 12-14, 2022
201. M. Omaña, F. Finelli, **C. Metra,** "Impact of Soft Errors on High Performance Autoencoders for Cyberattack Detection", in *IEEE Proceedings of the IEEE International Latin American Test Symposium*, Virtual Event, September 5-8, 2022
202. M. Zhupa, M. Naldi, M. Omaña, **C. Metra**, "On the Reliability of Clock Monitoring Units of Microcontrollers for Safety Critical Applications", in *IEEE Proc. of the 30th IEEE Int. Symp. on On-Line Testing and Robust System Design*, Rennes (France), July 3-5, 2024
203. S. Cretì, M. Omaña, **C. Metra**, G. Borellil, "Reliability of AI in Predicting the State of Health of Li-Ion Batteries", in *IEEE Proc. of the 30th IEEE Int. Symp. on On-Line Testing and Robust System Design*, Rennes (France), July 3-5, 2024
204. M. Omaña, A. Manfredi, **C. Metra**, R. Locatelli, M. Chiavacci, S. Petrucci, "Silent Data Corruption and Reliability Risks due to Faults Affecting High Performance Microprocessors' Caches", in *IEEE Proc. of the 30th IEEE Int. Symp. on On-Line Testing and Robust System Design*, Rennes (France), July 3-5, 2024

205. M. Omaña, F. Cantagallo, F. Finelli, **C. Metra**, "Reliability of AI for Cyberattack Detection in the Metaverse", in *IEEE Proc. of IEEE Int. Symposium on Emerging Metaverse*, Bellevue (WA), October 21, 2024

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