Curriculum Vitæ et Studiorum

Name	Andrea Bartolini
Date of birth	August 21, 1981
Citizenship	Italian
Affiliation	University of Bologna
	Dipartimento di Ingegneria dell'Energia Elettrica e dell'Informazione
Address	Viale del Risorgimento, 2, 40136 Bologna (BO) - Italy
	Phone: +39 051 209 3785
Email	a.bartolini@unibo.it
Web page	http://www-micrel.deis.unibo.it/ bartolini/
Affiliation	Swiss Federal Institute of Technology Zurich
	Institute of Integrated System
Address	Gloriastrasse 35, 8092 Zurich - Switzerland
	Phone: +39 051 209 3785
Email	andrea.bartolini@iis.ee.et
Web page	https://iis.ee.ethz.ch/portrait/staff/barandre.en.html

Short Bio

Since 2007, Andrea Bartolini has published (international, peer-reviewed) 14 journal papers (17 accepted) and 58 conference papers. Publications includes top IEEE and ACM journals. My h-index is 13, g-index is 18 (from Google Scholar, on January 29th, 2017). For a total of 552 citations count.

Andrea Bartolini has started his scientific research activity at Freescale Semiconductor LTD with focus on low-power and energy-efficient SW stack and Operating Systems for multimedia embedded platforms. During his PhD Andrea Bartolini has enlarged these research topics on cross-domains (embedded and high performance computing) multicore and many-core platforms, building his knowledge in architecture level performance and power modelling. During his stay at Intel Lab Germany he had chance to gain a more in depth understanding of Intel server platforms and many-core system SW stack, including the Linux O.S. power management and monitoring subsystem. Andrea Bartolini was an active member of the Intel Single Chip Cloud Computing community named MARC. During these years he started working on research projects involving strong algorithm knowledge in the control-theory, system identification and machine learning expanding his expertise in cross-cutting domains. During his post-doctoral research activities at UNIBO, he was involved in the preparation and implementation of the PHIDIAS FP7 FET project in which he gains the opportunity of learning advance knowledge in ultra-low power design and advance signal processing strategies. He has been involved in the preparation and implementation of the MULTITHERMAN ERC Advance project in which he is currently responsible for the activities on thermal and energy efficient design for high-performance computing systems. In the same years he has started a fruitful collaboration, with frequent visit, with CINECA the Italian supercomputer centre (hosting a Tier0 PRACE supercomputer and the November 2013 greenest supercomputer Eurora). Thanks to that he has gained in depth and practical knowledge of Supercomputers and High-Performance-Computing design, usage and challenges. Covering all the aspect from the application optimization till the system management and infrastructure design and planning.

Three years ago Andrea Bartolini moved in the Integrated System Institute in the D-ITET department at ETH Zurich. Maintaining a part-time position at the DEI department in UNIBO to follow the research col-

laboration with CINECA, the E4 Computer Engineering Company and the MULTITHERMAN ERC advance project. In Zurich he has started working and being responsible for two Nanotera project, the YINS project which targets energy-efficient server platform based on ultra-low power electronic techniques and the Ultrasound2Go which studies high-performance computing but energy efficient architecture for portable ultrasound imaging systems. In the YINS project he has experienced the combination of modelling strategies and many-core prototypes built on advance technology (i.e. FDSOI) for extracting coarse grain power, performance and thermal models of digital devices. In the Ultrasound2Go project he has experienced ASIC design for US2GO imaging. Since the last year he was involved as expert in the preparation of two FET4HPC project proposals which now have started (ANTAREX and EXANODE) with focus on HPC application reconfigurability and next Exascale node architecture. Andrea Bartolini is an expert member in the ETP4HPC for the definition of the European HPC agenda, and he has been involved as a consultant for E4 Computer Engineering with task in the energy-efficient design of future green HPC node. As a result of this effort, since June 2014 he is partner of E4 in the the PRACE-3IP Pre-Commercial Procurement tender targeting the co-design for energy-efficiency of a Petaflop supercomputer, and have contributed to the designed of one of first supercomputer based on ARMv8 manycore SoCs and accelerator cards in the project Phase II. In Phase III Andrea Bartolini is leading the activities for the design of the power management support of D.A.V.I.D.E. (Development for an Added Value Infrastructure Designed in Europe) which consists of an energy aware Petaflops class High Performance cluster based on IBM openpower architecture and nvidia pascal cards which is going to be installed in the first half of 2017 in Europe.

Since 2011 Andrea Bartolini is responsible for the research activities of a small team of PhDs students and research collaborators in the domain of energy-efficient and thermal-aware design strategies for a wide spectrum of computing platforms: ranging from ultra-low power embedded devices to large scale HPC systems. He is leading these activities as well as the collaborations with the different academic and industrial partners. Thanks to the strong industrial background and research focus Andrea Bartolini has received several awards for its research and technology transfer activities.

Contents

Position and Education

RECORD OF EMPLOYMENT

10/2013 – present

Postdoctoral fellow at the Institute of Integrated Systems (IIS) in the of Information Technology and Electrical Engineering (D-ITET) of the Swiss Federal Institute of Technology Zurich. (Reference *Prof. Luca Benini*).

04/2011 – present

Postdoctoral fellow at the Department of Electrical, Electronic and Information Engineering Guglielmo Marconi (DEI) Universit di Bologna, Italy. (Reference *Prof. Luca Benini*).

03/2015 - 04/2015

External Consultant for E4 Computer Engineering Spa Scandiano, Italy. *Responsible for the power management and monitoring as well as for the energy efficiency design in the Phase II PRACE-3IP PCP TENDER for the award of a Pre-Commercial Procurement contract concerning R&D services on Whole System Design for Energy Efficient HPC.* (Reference *Piero Alto*).

01/2014–06/2014

External Consultant for the European Exascale Software Initiative 2 n the WG5.5 on Disruptive technologies - NEOVIA (Reference *Giovanni Erbacci*)

07/2009–12/2009

Engineering Intern at Intel Germany Research Center GmbH of Intel Lab - Braunschweig, Germany (Reference *Matthias Gries*)

04/2007–12/2007

Software programmer and Linux Kernel developer at the Advanced Tecnology Group of Freescale Semiconductor Ltd Aylesbury, United Kingdom (Reference *Nigel Drew*)

EDUCATION

- Ph.D. in Electronic Engineering at Department of Electronics, Informatics and Computer Science (DEIS), University of Bologna, in 2011.
  Thesis Title: *Dynamic Resource Management: From portable devices to High Performance Computing*
  Advisor: *Prof. Luca Benini*

- *Laurea* Master degree in Electronic Engineering in 2007,110 (out of 110) cum laude
  Thesis title: *Analysis of the Memory Hierarchy of a SoC for multimedia applications*,
  Advisor: *Prof. Luca Benini*

VISITING EXPERIENCES

- Visiting researcher at HPC Group CINECA Bologna, Italy (March 2013 - September 2013). (Reference *Carlo Cavazzoni*).
- Visiting researcher at Electrical and Computer Engineering Department Boston University Boston, (MA) US (July-2012 to August-2012). (Reference *Ayse Kivilcim Coskun*)

Awards

AW.1. Gauss Award Winning as co-author of the paper ”Predictive Modeling for Job Power Consumption in HPC Systems” at ISC16 (June 2016, Frankfurt am Mann)

AW.2. Best Paper Award Nomination as co-author of the paper ”An Ultra-Low Power Dual-Mode ECG Monitor for Healthcare and Wellness” at DATE15 (March 2015, Grenoble)

AW.3. HiPEAC Technology Transfer Award for the work on ”Energy-Optimal workload allocation for micro-controller platforms based on heterogeneous multicores” in collaboration with NXP (HiPEAC Steering Committee,Dec 2014)

AW.4. Best IP Paper Award as co-author of the paper ”Thermal analysis and model identification techniques for a logic + WIDEIO stacked DRAM test chip” at DATE14 (March 2014, Dresden)

AW.5. Best Paper Award at DATE13 as co-author of the paper ”SCC thermal model identification via advanced bias-compensated least-squares” (March 2013, Grenoble)

AW.6. HiPEAC Technology Transfer Award for the work on ”Advance Energy/Thermal control techniques for supercomputer operating cost reduction” in collaboration with CINECA (HiPEAC Steering Committee,Dec 2013)

AW.7. HiPEAC Paper Award as co-author of the paper ”Workload and User Experience-Aware Dynamic Reliability Management in Multicore Processors” at DAC’13 (HiPEAC Steering Committee, 2013)

AW.8. NVIDIA POSTER AWARD as co-author of the poster ”An Ambient Temperature Variation Tolerance Scheme for ULP Shared-memory processor Cluster” @ 8th HiPEAC conference (Berlin, Jan 2013)

Professional Activities

Scientific Committees

- Expert member in the Engineer Board of Professional Practice and Ethics Examination Italy (2012)
- PhD Defense Committee Member, Escuela Tcnica Superior de Ingeniero de Telecomunicacin of the Universidad Politcnica de Madrid (June 2015)
- Expert Member of the ETP4HPC (SRA ENRE and SRA ARCH workgroup) 2015
- Expert Member of Energy and Power Aware Job Scheduling and Resource Management Team of EE HPC WorkGroup 2016/2017
- Expert Member at the Master’s Project Exam EPFL 2017

Contribution to Industrial Research Projects

- Co-PI in a collaboration grant with E4 Computer Engineering SpA for co-designing a peta-scale supercomputing system based on IBM openpower processor and NVIDIA P100 accelerator cards. Responsible for the design of the power management software stack and energy monitoring. Phase III

- Co-PI in a collaboration grant with E4 Computer Engineering SpA for co-designing next-generation green supercomputers based on ARM 64bit. Responsible for the design of the power management software stack and energy monitoring. Phase II
- Technical leader and main referent in the collaboration grant with CINECA computing center to develop new energy efficient run-time solution for the EURORA HPC Machine (1st in the Green500 July 2013) and next generation Exascale Supercomputer Machines.
- (Past) Technical leader in the collaboration grant with NXP Nederland on the design of next generation low-power heterogeneous microcontroller.
- (Past) Technical leader in the Intel Lab Single Chip Cloud Computer research project Next generation Energy and Thermal aware - Close-Loop Task Allocation and Dynamic Resource Management
- (Past) Technical leader in the collaboration grant with Intel Germany Microprocessor Lab on the topic of multicores resource management.
- (Past) Technical contributors in the collaboration grant with the Advance Technology Group of Freescale Semiconductor on the topic of dynamic luminance scaling algorithms for LCD energy optimization.

CONTRIBUTION TO NATIONAL AND INTERNATIONAL ACADEMIC RESEARCH PROJECTS

- WP coordinator and technical leader and proposal writer in the EU H2020 FET4HPC funded project AnTAREX (AutoTuning and Adaptivity appRoach for Energy efficient eXascale HPC systems)
- Technical leader and proposal writer in the EU H2020 FET4HPC funded project EXaNoDe (European Exascale Processor Memory Node Design)
- WP coordinator and technical leader in the ERC Advance funded project MULTITHERMAN (MULTI-scale THERmal MANagement of Computing Systems)
- Technical leader in the Swiss nano-tera.ch YINS (Developing a radically new thermal-aware design approach for next generation energy-efficient datacenters)
- (Past) Technical contributor in the Swiss nano-tera.ch Ultrasound To Go for the design of portable ultrasound medical devices.
- (Past) WP coordinator and technical leader and proposal writer in the FP7 EU funded project PHIDIAS (Ultra-Low-Power Holistic Design for Smart Bio-signals Computing Platforms)
- (Past) Sub-contractor in the FP7 EU funded project THERMINATOR (Modeling, Control and Management of Thermal Effects in Electronic Circuits of the Future)

SCIENTIFIC COLLABORATIONS (BEYOND EU-PROJECTS)

- Lawrence Livermore National Laboratory- USA (2017 - ongoing)
  Contact Person: Tapasya Patki
  Topic: Simulating Infrastructure for Power Capping
- E4 Computing Engineering - Italy (2015 - ongoing)
  Contact Person: P. Altoe, F. Magugliani
  Topic: Design and support for energy-efficiency in next-generation supercomputing node
- University of Cambridge - Cambridge Data Centre (2015- ongoing)
  Contact Person: Filippo Spiga
  Topic: Energy-efficiency APIs and Scientific Applications

- POLIMI - Politecnico di Milano - Italy (2015 - ongoing)
  Contact Person: Cristina Silvano, Gianluca Palermo, Giovanni Agosta
  Topic: Integration of scalable monitoring framework and autotuning services in HPC systems
- IMEC - Interuniversity Micro-Electronics Centre - The Netherlands (2014 - ongoing)
  Contact Person: Tobias Gemmeke
  Topic: Novel Memory Design and Characterization for Energy-Efficient Biosensing Node
- NXP-Eindhoven - The Netherlands (2013-2015)
  Contact Person: Jose Pineda de Gyvez
  Topic: Energy-Efficient Parallel Micro-controller Design
- EPFL - Ecole Polytechnique Fdrale de Lausanne - Switzerland (2012-ongoing)
  Contact Person: D. Atienza
  Topic: Energy-efficient architectures
  Contact Person: B. Falsafi
  Topic: Scale-out computing nodes based on FD-SOI technology and ARMv8 cores.
  Contact Person: P. Vandergheynst
  Topic: Approximate Compressive Sensing.
  Contact Person: F. Angiolini
  Topic: Portable Ultrasound Medical devices.
- CINECA - SuperComputing Applications and Innovation Department, Italy (2012-ongoing)
  Contact Person: Carlo Cavazzoni, Nico Sanna
  Topic: Energy-efficient supercomputing systems.
- Eurotech - (2014)
  Contact Person: G. Tecchiolli
  Topic: Eurora and Aurora energy and thermal efficiency.
- UNIBO - University of Bologna (2010 - ongoing)
  Contact Person: Roberto Rovatti, Mauro Mangia
  Topic: Rakeness based compressive sensing nodes.
  Contact Person: Michela Milano, Michele Lombardi
  Topic: Artificial Intelligence methods for smart resource management
  Contact Person: Roberto Diversi, Andrea Tilli
  Topic: Advance thermal control and modelling of electronic devices.
  Contact Person: Andrea Lodi
  Topic: ILP modelling of thermal control problem for multicore systems
- INFN-SISSA - Scuola Internazionale Superiore di Studi Avanzati - Trieste Italy (2015)
  Contact Person: Stefano Cozzini
  Topic: Energy Monitoring and Characterization of the Aurora Computing Node
- BU - Boston University (2011-ongoing)
  Contact Person: Ayse Coskun
  Topic: Energy-efficient manycore systems modelling
- Intel Germany Research Center GmbH Intel Lab - Braunschweig, Germany (2009-2013)
  Contact Person: Matthias Gries
  Topic: Manycore/Single Chip Cloud Computer (SCC) dynamic resource management

- Freescale Semiconductor Ltd Advanced Technology Group Aylesbury, United Kingdom (2007-2009)
  Contact Person: Nigel Drew
  Topic: Energy Saving Algorithm in the O.S. of mobile/multimedia SoC

CONFERENCE AND WORKSHOP ORGANIZATION

Program Chair and Organization Committees

- WEHA (2016,2015,2014) - International Workshop on Energy-aware high performance Heterogeneous Architectures and Accelerators - *Workshop Organizer*
- DATE (2017,2016,2015,2014) - Design Automation and Test in Europe - *Session Chair*
- ISLPED (2015) - International Symposium on Low Power Electronics and Design - *Session Chair*
- NOCS (2014) - International Symposium on Networks-on-Chip - *Web Chair*

Program Committee Membership

- DATE (2014 -2015,2017) - Design Automation and Test in Europe
- EUC (2005, 2014 - 2015) - International Conference on Embedded and Ubiquitous Computing
- PATMOS (2015,2014,2013) - International Workshop on Power And Timing Modeling, Optimization and Simulation
- VLSI-SoC (2017) - IFIP/IEEE International Conference on Very Large Scale Integration

REFEREE SERVICES IN JOURNALS AND CONFERENCES

- *Conferences and Workshops*: DAC - Design Automation Conference, DATE - Design Automation and Test in Europe, PATMOS - International Workshop on Power and Timing Modelling, EUC - Embedded and Ubiquitous Computing, ISCAS - International Symposium on Circuits and Systems, VLSI-SoC - IFIP/IEEE International Conference on Very Large Scale Integration
- *Journals*: IEEE Transaction on Computer, IEEE Transaction on Parallel and Distributed Systems, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, IEEE to Design and Test of Computers, Elsevier Integration, the VLSI Journal, ACM Embedded Systems Letters, IEEE Transactions on Sustainable Computing, IEEE Design & Test

Teaching Activities

2015

Lecturer at the Master in High Performance Computing at SISSA Trieste,
Introduction to Computer Architectures for HPC, lecture module: *"Trends in Energy, Power and Thermal Efficiency of HPC systems*" - ICTP/SISSA Trieste, Italy (Oct. 2015)

2015

Lecturer at the Master-Level PRACE Advanced School on Parallel Computing,
lecture module: *"Energy Efficient Programming*" - CINECA Bologna

2014

Lecturer at the Master-Level PRACE Advanced School on Parallel Computing,
lecture module: *"Energy Efficient Programming*" - CINECA Bologna

2012

Lecturer at the Advanced school on ICT for Future Energy Systems,
lecture module: *"Thermal-Aware Design for Energy-Efficient Multi-Core Systems and Datacenters*" - Trento (Sept 2012)

2015-2016

Teaching Assistant in the Electronics Engineering Degree program of University of Bologna, Italy
Hardware-Software Design of Embedded Systems, IV year, curriculum Electronics and Informatics, AA 2014/15, 2015/2016
MS Final Project supervisor

2008-2011

Teaching Assistant in the Electronics Engineering Degree program of University of Bologna, Italy
Hardware-Software Co-design, IV year, curriculum Electronics and Informatics, AA 2008/09, 2009/10, 2010/11
MS Final Project supervisor

2008-2011

Teaching Assistant in the Informatics Engineering Degree program of University of Bologna, Italy
Electronics, III year, fundamentals, AA 2008/09, 2010/11.
BS Final Project supervisor

2011-2012

BS Final Project supervisor in the Informatics Engineering Degree program of University of Bologna, Italy:
Artificial Intelligence Applications, V year, thermal modeling, AA 2010/2011, 2011/2012.

INVITED LECTURERS

Invited Booth Presenter at EEHPC Booth in Supercomputing 2016 - Salt Lake City, USA (Nov. 2016)

Invited Lecturer at the ARM Research Summit 2016, *ARMv8-based Computing Cluster: Co-Design for Energy-Efficiency and Monitoring* - Cambridge, UK (Sept. 2016)

Invited Presentation at the International Workshop of Dynamic Code Auto-Tuning at the 2016 Symposium on Code Generation and Optimization (CGO), *Trends in Energy and Thermal efficiency of High Performance computing infrastructure* - Barcellona, Spain (March. 2016)

Invited Lecturer at the Dagstuhl Seminar 16052, *Dark Silicon: From Embedded to HPC Systems* - Dagstuhl Schloss, Germany (Jan. 2016)

Invited Lecturer at the Workshop on Computational Science Infrastructure and Applications for Academic Development in the ICTP, "*Trends in Energy, Power and Thermal Efficiency of HPC systems*" - ICTP Trieste, Italy (Oct. 2015)

Invited Lecturer at ICT-Energy Summer School, "*Energy management policy for ultra-low power devices*" -Perugia (Jul. 2014)

Invited Booth Presenter at Intel European Research & Innovation Conference (ERIC) 2011 - Leixlip, Ireland (Oct. 2011)

STUDENTS' SUPERVISION

PhDs Students Supervision/Co-Advisor

- Daniele Cesarini, PhD student@UNIBO (2016–ongoing)
  Thermal-aware programming methodologies - ANTAREX,MULTITHERMAN,CINECA;
- Pascal Hager, PhD student@ETHZ (2014–2015)
  Low-power medical ultrasound and beamforming architectures Ultrasound-To-Go;
- Francesco Beneventi, research assistant (2011–ongoing)
  Thermal modelling and monitoring of large scale infrastructures, MULTITHERMAN,CINECA,E4;
- Daniele Bortolotti, PhD student@UNIBO (2013–2016)
  Low power biosensing node architectures and energy-efficiency APIs, PHIDIAS, E4;
- Thomas Bridi, PhD student@UNIBO (2015–ongoing)
  Scalable supercomputing resource management, MULTITHERMAN,CINECA;
- Andrea Borghesi, PhD student@UNIBO (2014–ongoing)
  Supercomputer Power Capping, MULTITHERMAN, CINECA;
- Antonio Libri, PhD student@ETHZ (2016–ongoing)
  Distributed monitoring of computing nodes, ANTAREX,E4
- Piero Mercati, PhD student@UCSD (2014–2016)
  Dynamic reliability management, MULTITHERMAN
- Christian Pinto, PhD student@UNIBO (2015)
  Modelling strategies for Heterogeneus Computing Nodes - YINS,MULTITHERMAN

Graduate Students Supervision/Co-Advisor

- Master Thesis supervisor (4 thesis) DEI Universit di Bologna. Italy
- Master Thesis supervisor (1 thesis) Swiss Federal Institute of Technology in Zurich, Switzerland.
- Master Project supervisor (1 thesis) Swiss Federal Institute of Technology in Zurich, Switzerland

Research Interests

My main research focus is on energy-efficient design of electronic devices ranging from ultra-low power embedded systems to large scale High-Performance Computing infrastructures. In particular, I am interested in: (i) modelling of the physical effects which are at the basis of the energy-consumption of electronic devices as well as the physical effects induced by their power consumption. In this domain I am interested in computer-aided methodologies to make these physical models tractable and empirically tunable on targets devices; (ii) Optimization methodology, algorithms and strategies suitable to embed rules and models directly on the target system and to generate an optimal usage of the hardware resources w.r.t. specific target metrics. (iii) The design of novel architectures for the software components as well as of the hardware extensions needed for implementing self-learning and self-optimizing control loops in the target electronic devices. (iv) The study of novel cross-boundary (in between Hardware and Software) methodologies to create opportunities for a deeper energy-and-performance efficient usage of the final device as well as the application of these methodologies in the design of novel cutting-edge energy-efficient computing systems.

(I) Energy/Power/Thermal Modelling of Computing Devices

Energy-efficiency is a primary concern in the design of a wide range of electronic devices. At the technological layer, the heat generated by the power consumed by the transistors integrated in the silicon die needs to be removed to avoid thermal issues. This limits the peak clock frequency as well as the number of resources which can be safely powered at the same time. At system level several components contribute to the overall power consumption in addition to the computing engine. Significant power is spent in ultra-low-power monitoring devices by the wireless communication and data transfer, in multimedia devices by the display, and in large scale high-performance computing installation by the cooling system. The different hardware components expose control knobs capable of modulating the power consumption at the cost of reduced performance or functionalities. When seen from the user and application perspective the raw hardware performance are not representative of the final QoS as effect of workload phases and users perception. It is thus important to evaluate the effect of these control knobs in terms of physical quantities (power, energy, temperature) and application performance.

The contribution in this field has been the creation of tools and methodologies for modelling the power consumption and the energy-efficiency as well as the thermal dissipation of different HW architectures and systems. This has been done with both synthetic and realistic workloads with the goal of creating physically-valid model templates suitable to be handled by control/optimization loops or being analytically solved. In this field I have studied scalable algorithms for the stress and automatic learning of these models. Me and my-collaborators were among the firsts in showing the benefit of system identification strategies [JR.14],[JR.13], [JR.17],[IC.36] as well as neural-networks [JR.6], [IC.44] and regression trees for several computing segments [IC.7]. These approaches have led to several recognitions (DATE13 BP Award [AW.5], DATE14 IP Award [AW.4], ISC16 Gauss Award)[AW.1] .

(II) Optimization Methodology for resource management

To improve the energy-efficiency of the target electronic device, on-line resource management techniques aim to adapt the hardware performance to the application and user requirements. However finding the best operating point for a given workload using a reactive ”try-and-test” approach is suboptimal. Moreover it cannot ensure a target performance level and cannot guarantee energy-saving for all the applications.

The contribution in this field has been the integration of modelling strategies with optimization frameworks (ILP, Convex optimization) and formal control methodologies, such as the Model Predictive Control, to create predictive resource management techniques characterized by low-overhead and scalable topologies [JR.17],[IC.52][JR.11].

(III) Resource management run-time architectures

When bringing these strategies in the real system several HW and SW components need to be rethought and adapted. When taking at example a supercomputer system, optimizing its run-time behaviour implies touching the operating system, the programming library, the job dispatcher as well as the node and room cooling policy. Each of these components is characterized by its own complexity and software architecture. Moreover the creation of the communication channels in between all these components needs to satisfy the constraints in security and reliability of the final system.

The contributions in this field have been the design of novel monitoring framework at the operating system and user level [IC.25],[IC.30], the design of novel reliability-aware governors at operating-system level [IC.40],[IC.23],[IC.10], the design of novel job dispatcher and scheduling algorithm as a plug-in component for commercial solutions [JR.7] as well as the design of novel cooling control strategies for advance and hybrid cooling infrastructures [IC.14],[IC.19],[JR.5].

(IV) Cross-Boundary and Cutting-Edge Energy-Efficient Computing Systems

The co-design of the target application, system and computing architecture creates novel opportunities for achieving deeper energy efficiency. I have focused my interest in two systems: bio-sensing/monitoring nodes based on parallel processors and advance technologies as well as high-performance computing nodes based on novel technologies and architectures. The contribution in the first domain has been the extension of standard low-power methodologies such as near-threshold computing by introducing hybrid memory design suitable to operate the node at lower voltages and trading off sensing quality w.r.t. a deeper energy-efficiency[IC.11],[IC.28]. In the same domain I have studied the usage of compressive sensing approaches to reduce the energy dissipated during the data transmission in ECG monitoring [JR.3],[IC.29], [IC.28],[IC.18],11. When the monitored data are visualized on a smartphone with a display I have studied dynamic approaches to reduce the energy-consumed by the display [IC.55],[IC.56]. Finally when moving to high-performance computing nodes the contributions have been the evaluation and introduction of scale-out computing nodes based on ARMv8 many-core SoCs manufactured in advance technology nodes and operating in near-threshold domain as well as the design of novel operating system level and programming model support for novel energy-efficient directives and their evaluation in real scientific applications [IC.12], [JR.10]. I have designed fine grain energy monitoring in an industrial prototype based on upcoming ARMv8 SoCs [IC.6]. Currently I am involved in an industrial project in partnership with E4, Wistron, IBM and NVIDIA and CINECA on the co-design for energy efficiency of the first petascale supercomputer based on openpower architecture and nvidia pascal GPUs and dedicated energy-management support.

Publication List

JR.1. R. Braojos; D. Bortolotti; A. Bartolini; G. Ansaloni; L. Benini; D. Atienza; ”A Synchronization-Based Hybrid-Memory Multi-Core Architecture for Energy-Efficient Biomedical Signal Processing” in IEEE Transactions on Computers , vol.PP, no.99, pp.1-1 doi: 10.1109/TC.2016.2610426 (Accepted for Pubblication)

JR.2. P. Mercati; F. Paterna; A. Bartolini; L. Benini; T. Rosing; ”WARM: Workload-Aware Reliability Management in Linux/Android,” in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems , vol.PP, no.99, pp.1-1 doi: 10.1109/TCAD.2016.2611501 (Accepted for Pubblication)

JR.3. Bortolotti D.; Mangia M.; Bartolini A.; Rovatti R.; Setti G.; Benini L.; ”Energy-Aware Bio-signal Compressed Sensing Reconstruction on the WBSN-gateway” IEEE Transactions on Emerging Topics in Computing, doi: 10.1109/TETC./-2016.2564361 (Accepted for Pubblication)

JR.4. Bortolotti D.; Bartolini, A.; Benini L.; ”Zeroing for HW-efficient Compressed Sensing Architectures Targeting Data Compression in Wireless Sensor Networks Microprocessors and Microsystems”, in Microprocessors and Microsystems, Volume 48, February 2017, Pages 69-79, ISSN 0141-9331, http://dx.doi.org/10.1016/j.micpro.2016.09.007. Elsevier

JR.5. Conficoni C.; Bartolini A.; Tilli A.; Cavazzoni,C.; Benini L.; ”Integrated Energy-Aware Management of Supercomputer Hybrid Cooling Systems” in IEEE Transactions on Industrial Informatics , vol. 12, no. 4, pp. 1299-1311, Aug. 2016. doi: 10.1109/TII.2016.2569399

JR.6. Michele Lombardi, Michela Milano, Andrea Bartolini, ”Empirical decision model learning”, Artificial Intelligence, Available online 13 January 2016, ISSN 0004-3702, http://dx.doi.org/10.1016/j.artint.2016.01.005.

JR.7. T. Bridi; A. Bartolini; M. Lombardi; M. Milano; L. Benini, ”A Constraint Programming Scheduler for Heterogeneous High-Performance Computing Machines,” in IEEE Transactions on Parallel and Distributed Systems, vol. 27, no. 10, pp. 2781-2794, Oct. 1 2016. doi: 10.1109/TPDS.2016.2516997

JR.8. Beneventi F.; Bartolini A.; Vivet P.; Benini L.; ”Thermal Analysis and Interpolation Techniques for a Logic + WideIO Stacked DRAM Test Chip”, in Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, vol. 35, no. 4, pp. 623-636, April 2016. doi: 10.1109/TCAD.2015.2474382

JR.9. Hager P.A.; Bartolini A.; Benini L.; ”Ekho: A 30.3W, 10k-Channel Fully Digital Integrated 3-D Beamformer for Medical Ultrasound Imaging Achieving 298M Focal Points per Second”, in Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, Year: vol. 24, no. 5, pp. 1936-1949, May 2016. doi: 10.1109/TVLSI.2015.2488020

JR.10. Davide Rossi, Antonio Pullini, Igor Loi, Michael Gautschi, Frank K. Grkaynak, Andrea Bartolini, Philippe Flatresse, Luca Benini, ”A 60 GOPS/W, -1.8 V to 0.9 V body bias ULP cluster in 28 nm UTBB FD-SOI technology”, Solid-State Electronics, Volume 117, March 2016, Pages 170-184, ISSN 0038-1101, http://dx.doi.org/10.1016/j.sse.2015.11.015.

JR.11. A. Tilli, A. Bartolini, M. Cacciari, L. Benini; ”Guaranteed Computational Resprinting via Model-Predictive Control”, in Transactions on Embedded Computing Systems (TECS) Special Issue on Embedded Platforms for Crypto and Regular Papers, Volume 14 Issue 3, Article No. 48, DOI: 10.1145/2724715, ACM New York, NY, USA, May 2015

JR.12. M. Sadri, A. Bartolini, L. Benini; ”Temperature variation aware multi-scale delay, power and thermal analysis at RT and gate level”, in Integration, the VLSI Journal, Volume 49, March 2015, Pages 3548, DOI: 10.1016/j.vlsi.2014.10.005, Elsevier 2015 **(**> 10 **Citations)**

JR.13. Beneventi F. ; Bartolini A. ; Tilli A. ; Benini L., ”An Effective Gray-Box Identification Procedure for Multicore Thermal Modeling”, in: Computers, IEEE Transactions on (Volume:63 , Issue: 5), Page(s): 1097 1110, ISSN :0018-9340, DOI: 10.1109/TC.2012.293, 2014 IEEE **(**> 10 **Citations)**

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