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Antonio del Vecchio

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ABOUT MYSELF

Ph.D. student in the Electronic Engineering program at the University of Bologna, specializing in Power Management for Edge Computing and HPC RISC-V systems. Experienced in the design and development of hardware and firmware for embedded systems, with proficiency in various programming languages.
Passionate about drone building and testing.

EDUCATION AND TRAINING

[01/11/2022 – Current] **PhD in Electronic Engineering**

Alma mater studiorum, Università di Bologna

City: Bologna | **Country:** Italy |

[2017 – 2022] **Master's degree in Electronic Engineering**

Alma mater studiorum, Università di Bologna

City: Cesena | **Country:** Italy |

Relevant achievements of the course:

- Advanced knowledge in computer architectures and HPC.
- Study of embedded thermal and power management systems.
- Experience in SystemVerilog programming.
- Knowledge and experience in design validation methods and tools (e.g., Questasim).
- Experience with Linux system for embedded architectures.
- Experience in Git control system.

[2013 – 2017] **Bachelor's degree in Electronic Engineering**

Alma mater studiorum, Università di Bologna

City: Cesena | **Country:** Italy |

Relevant achievements of the course:

- Study and development of firmware for embedded systems in C and C++ languages.
- Knowledge of the use cases of the main computing architectures.
- In depth study of the main communication protocols of digital systems.
- Knowledge and use of FPGA hardware based boards for RTL network development.
- Study of computer architecture fundamentals and RISC assembly language.

LANGUAGE SKILLS

Mother tongue(s): Italian

Other language(s):

English

LISTENING B2 **READING** B2 **WRITING** B2

SPOKEN PRODUCTION B2 **SPOKEN INTERACTION** B2

Levels: A1 and A2: Basic user - B1 and B2: Independent user - C1 and C2: Proficient user

SKILLS

Languages

SystemVerilog | VHDL | C | C++ | Python | Java | Assembly | MATLAB

Operating Systems

Linux | Windows

IDEs and other tools

Xilinx Vivado | Electric VLSI | Intel Quartus | Questasim | KiCad | Eagle CAD | Simulink

Others

RaspberryPi | LaTeX | ARM mbed | STM32CubeIDE | Betaflight Configurator | Arduino

EDUCATIONAL EXPERIENCES

[01/04/2025 – Current] **Research Internship at ETH Zurich Integrated Systems Laboratory**

Conducted research on hardware and software platforms for predictive and mixed-critical applications in the context of real-time power management for High Performance Computing systems.

Focused on the ControlPULP open-source RISC-V based hardware platform, extending its capabilities for:

(i) predictability in real-time workloads,

(ii) acceleration of advanced control algorithms such as Model Predictive Control (MPC),

(iii) optimization of MPC algorithm execution on custom-developed hardware, and

(iv) porting the XRCE middleware to the newly developed ControlPULP platform version.

[01/05/2024 – 01/11/2024] **Research Internship at Leonardo Labs**

Conducted research in the Deep Digital Technologies area at Leonardo Labs, with a primary focus on the following topics:

Evaluation of performance monitoring tools and energy consumption for the company's HPC infrastructures.

Study and utilization of architectures, accelerators, and software ecosystems developed for RISC-V technologies in Edge Computing for industrial applications.

[03/06/2024 – 07/06/2024] **ETH Future Computing Laboratory (EFCL) 2024 Summer School**

Participated in the EFCL Summer School, with a focus on the "Customizing RISC-V Based Microcontrollers" track.

It provided a hands-on session on customizing a RISC-V core for DSP/FIR extension.

[25/09/2023 – 29/09/2023] **Training at Esperanto Technologies**

Attended a week-long educational training session at Esperanto Technologies, covering the software stack and hardware aspects of their AI accelerator based on the System On Chip ET-SoC-1.

[01/09/2023 – 01/09/2024] **Laboratory Tutor for C programming course**

Undertook the role of laboratory tutor for the Fundamentals of Computer Science course, specifically focusing on C programming, for one year duration at UniBo, Bologna Campus.

[09/07/2023 – 15/07/2023] **ACACES 2023 Summer School**

Participated in International Summer School on Advanced Computer Architecture and Compilation for High-performance Embedded Systems (ACACES), where I attended the following courses:

- RISC-V vector CPU for High-Performance Computing by Filippo Mantovani, Barcelona Supercomputing Center;
- Energy-efficient and intelligent IoT devices by Michele Magno, ETH Zürich;
- Machine Learning for Microarchitectural Prediction by Daniel A. Jiménez, Texas A&M University;
- A gentle introduction to Quantum Computing Logic and Quantum Computers by Koen Bertels, QBee.

MAIN UNIVERSITY PROJECTS

VLSI design of a 4-bit accumulator

Development and analysis of a 4-bit digital accumulator in integrated CMOS technology.

Employed technologies:

- Utilized software: Electric VLSI
- LTspice

Atari Lunar Lander VHDL porting

VHDL porting of the famous 70's arcade game based on Intel Cyclone II FPGA chip.

Employed technologies:

- Utilized hardware: Terasic DE2 board, VGA enabled monitor
- Languages: VHDL
- Other tools: Quartus

Bachelor's degree thesis project

Interfacing an embedded system to a semantic platform for IoT application development via WebSocket connection.

Employed technologies:

- Utilized hardware: NUCLEO-F411RE STM board, STM32 X-NUCLEO IDW01M1 WiFi module
- Languages: C, C++
- Other tools: Mbed, STM32CubeIDE

Master's degree thesis project

FPGA prototyping of RISC-V based integrated subsystems for power management.

Contributions:

- Design end integration of SCMI support in ControlPULP platform:
  - Development of hardware support for SCMI Mailbox
  - Development of Mailbox driver and SCMI firmware for message handling in ControlPULP

    - ControlPULP SCMI firmware performance optimization inspired by ARM SCP message decoding mechanisms
- Validation and characterisation:
    - Testbench development and RTL simulation
    - FPGA emulation on Xilinx Ultrascale+

Employed technologies:

- Hardware: Zynq UltraScale+ MPSoC ZCU102 evaluation board
- Languages: C, C++, SystemVerilog, Assembly
- Other tools: Vivado, Questasim, PetaLinux

MAIN PROFESSIONAL PROJECTS

DDS generator for AC motor control

Development of a FPGA based Direct Digital System for speed control of an AC induction motor.

Employed technologies:

- Utilized hardware: Arty A7: Artix-7 FPGA development board
- Languages: VHDL, MATLAB
- Other tools: Vivado

Smart lighting control system

Hardware and firmware development of a microcontroller based custom board for smart lighting control.

Employed technologies:

- Utilized hardware: ATmega328, TL4242, HC-SR04,
- Languages: C, MATLAB
- Other tools: Atmel Studio, EagleCAD

Continuity tester for automotive bus

Hardware and firmware development of a modular continuity tester for automotive bus wires.

Employed technologies:

- Utilized hardware: ATmega2560
- Languages: C
- Other tools: Atmel Studio, EagleCAD

Composite materials oven control system

Hardware and firmware development of a control system for composite materials curing ovens.

Employed technologies:

- Utilized hardware: ATmega4809
- Languages: C
- Other tools: MPLAB, EagleCAD

AC motor end-of-line tester

Firmware development for an AC motor diagnostic machine, enabling real-time monitoring of current and temperature values during end-of-line testing.

Employed technologies:

- Utilized hardware: ATmega328
- Languages: C
- Other tools: Visual Studio Code

DATA: 23/05/2025