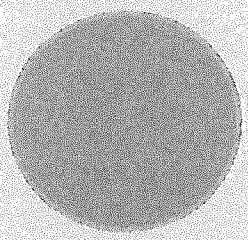
europass



Giovanni Bambini

Date of birth: 09/03/1994 | **Nationality:** Italian

WORK EXPERIENCE

01/11/2021 – CURRENT Bologna, Italy

PHD STUDENT ALMA MATER STUDIORUM - UNIVERSITÀ DI BOLOGNA - DEI

Researching HPC processors modeling and control architectures.
Developing HPC simulation framework on Matlab, including thermal model, power model, performance model, workload trace generation, discrete-time simulation, and control emulation.
Advancing MPC thermal and power control on HPC processors.
Developing firmware for a RISC-V thermal and power controller for HPC processors.
Working for EPI Rhea1 and Rhea2 European projects

30/04/2020 – 31/10/2021 Bologna, Italy

RESEARCH ASSOCIATE ALMA MATER STUDIORUM - UNIVERSITÀ DI BOLOGNA - DEI

Analysis and Development of a thermal and power controller for multicore HPC processors inside the European project EPI (https://www.european-processor-initiative.eu/project/epi/)
Development of an FPGA simulation framework for the hardware-software co-design of the above-mentioned processor controller.

EDUCATION AND TRAINING

08/2016 – 10/03/2020 Bologna, Italy

MASTER'S DEGREE IN AUTOMATION ENGINEERING ALMA MATER STUDIORIUM - University of Bologna

System Theory and Advanced Control
Mechatronics Systems Modeling and Control
Discrete Time Systems Identification and Control
Diagnosis and Control
Real Time Systems for Automation
Hardware-Software Design of Embedded Systems
Image Processing and Computer Vision
Industrial Robotics
Automation Software and Design Patterns
Mechanics of Machines for Automation

Website https://corsi.unibo.it/2cycle/AutomationEngineering | **Field of study** Automation Engineering | **Final grade** 102/110 |

Level in EQF EQF level 7 | **Type of credits** CFU | **Number of credits** 120 |

Thesis Design and Prototyping of a FreeRTOS-based Power Control Firmware for HPC Processors in GAP8

09/2013 – 19/12/2016 Bologna, Italy

BACHELOR'S DEGREE IN INGEGNERIA DELL'AUTOMAZIONE ALMA MATER STUDIORIUM - University of Bologna

Mathematics and Linear Algebra
Physics
Computer Science
Mechanics
Electronics
Combinatorial Network Theory
Automation Control

2022

Modeling the Thermal and Power Control Subsystem in HPC Processors

Abstract: [...] This paper provides a mathematical model of an HPC processor and the different control approaches implemented in state-of-the-art PCS solutions. In particular, we are comparing the performance of a custom cascade model-based control algorithm that favors cores executing more demanding workloads with the IBM Power9 control algorithm used as a reference design. [...]

G. Bambini, C. Conficoni, A. Tilli, L. Benini, A. Bartolini

2024

Modeling and Controlling Many-Core HPC Processors: an Alternative to PID and Moving Average Algorithms

Abstract: [...] To close the gap, in this work, we first provide a detailed thermal and power model targeting a modern High Performance Computing (HPC) MPSoC. We consider real-world coupling effects such as actuators' non-idealities and the exponential relation between the dissipated power, the temperature state, and the voltage level in a single processing element. We analyze how these factors affect the control algorithm behavior and the type of challenges that they pose. Based on the analysis, we propose a thermal capping strategy inspired by Fuzzy control theory to replace the state-of-the-art PID controller, as well as a root-finding iterative method to optimally choose the shared voltage value among cores grouped in the same voltage domain. We evaluate the proposed controller with model-in-the-loop and hardware-in-the-loop co-simulations. We show an improvement over state-of-the-art methods of up to 5x the maximum exceeded temperature while providing an average of 3.56% faster application execution runtime across all the evaluation scenarios.

G. Bambini, A. Ottaviano, C. Conficoni, A. Tilli, L. Benini, A. Bartolini

2020

An Open-Source Scalable Thermal and Power Controller for HPC Processors

Abstract: In the last decade, high performance multi-core processor designs have followed an increase in number of cores, interfaces, heterogeneity and System-on-chip (SoC) complexity. HPC applications also require tailored chip designs with specific operating points and performance indexes. In this scenario, an advanced and configurable Power Controller System (PCS) is necessary to meet power and thermal constraints, without the necessity of static ultra-conservative margins on the operating points [...]

G. Bambini, R. Balas, C. Conficoni, A. Tilli, L. Benini, S. Benatti, A. Bartolini

2022

ControlPULP: A RISC-V Power Controller for HPC Processors with Parallel Control-Law Computation Acceleration

Abstract: High-Performance Computing (HPC) processors are nowadays integrated Cyber-Physical Systems requiring complex and high-performance closed-loop control strategies for efficient power and thermal management. To satisfy high-bandwidth, real-time multi-input multi-output (MIMO) optimal power control requirements, high-end processors integrate on-die Power Controller Systems (PCS). [...]

A. Ottaviano, R. Balas, G. Bambini, C. Bonfanti, S. Benatti, D. Rossi, L. Benini, A. Bartolini

PROJECTS

05/10/2023 – CURRENT

HPC Modellig and Control Framework - AechPeSi Lab

Main Developer of an Open-Source project to model HPC processors and simulate different types of DVFS controllers.

The project consists of a series of MATLAB classes to model the thermal and power behavior of cores and chiplets, as well as application execution. Additionally, it includes classes to model DVFS controller algorithms, such as PID, Heuristic, and MPC. A script is used to carry out simulations, data analysis, and plotting result figures to compare execution metrics.

Link https://github.com/Ev3nt1ne/AechPeSi_lab

01/11/2022 – CURRENT

HW/SW Co-design HPC Framework

Main Developer of an Open-Source project to develop the Hardware, Firmware, and Control of HPC DVFS Thermal and Power controllers.