europass

Mattia Sinigaglia

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WORK EXPERIENCE

01/03/2024 – 30/09/2024 Bologna, Italy

UNIVERSITY TEACHING ASSISTANT UNIVERSITY OF BOLOGNA

Preparation and evaluation of laboratory exercises for the Master's degree course Hardware Software Design of IoT Systems - 93322 held by Professor Luca Benini. The exercises are designed to teach and apply parallel programming techniques using a multicore RISC-V-based architecture. The primary objective is to equip students with hands-on experience in developing and optimizing software on advanced platforms tailored for IoT systems.

Business or Sector Professional, scientific and technical activities | **Department** Computer Science and Electronic Engineering |

Email mattia.sinigaglia5@unibo.it | **Website** https://www.unibo.it/sitoweb/mattia.sinigaglia5/didattica/2023

01/11/2021 – 31/10/2022 Bologna, Italy

RESEARCH ASSISTANT IN UNIVERSITY UNIVERSITY OF BOLOGNA

Integration and testing of digital peripherals in System-on-Chip designs based on the RISC-V PULP architecture. The integration was implemented at the RTL level using the SystemVerilog language and the ModelSim simulation environment. Functional verification was subsequently completed through FPGA implementations, ensuring the correct operation of the peripherals within a Hardware-in-the-Loop setup.

Business or Sector Professional, scientific and technical activities |

Department Department od Electrical, Electronic and Information Engineering "Guglielmo Marconi" - DEI |

Email mattia.sinigaglia5@unibo.it | **Website** https://www.unibo.it/sitoweb/mattia.sinigaglia5/

01/10/2017 – 31/08/2018 Villanova Di Castenaso, Bologna, Italy

EMBEDDED SYSTEMS SOFTWARE DEVELOPER BLUEBERRY TECH S.R.L

I spearhead the development of a parking system project on the Raspberry Pi 3, featuring a web server accessible via Ethernet/Wi-Fi for configuration purposes. Collaborating closely with electronic engineers, we conceptualized and executed the software system from the ground up, aligning it with predefined functionalities.
Key Contributions:

- Engineered and developed the database architecture for the parking system.
- Designed and implemented a web server for system configuration.
- Crafted and programmed the firmware to ensure seamless operation
- Testing and product validation

EDUCATION AND TRAINING

01/11/2022 – CURRENT Bologna, Italy

PH.D STUDENT IN ELECTRONIC ENGINEERING University of Bologna

Ph.D. in Electronic Engineering under Professor Davide Rossi and Luca Benini's supervision, specializing in developing heterogeneous energy-efficient RISC-V-based SoCs. Expertise includes RTL design, IPs integration, FPGA prototyping, front-end ASIC synthesis, Physical Implementation, and performance validation. Moreover, I have expertise in PCB design for low-speed peripherals verification and chip bring-up.

- Contributed to the tape-out of Shaheen's SoC (GlobalFoundries 22nm) development. Shaheen is an IoT processor that couples a 64-bit Linux-capable RV64 core with a programmable accelerator of 8 RV32 cores. Managed the integration and verification of peripheral subsystems, developed low-level firmware, conducted peripheral testing on FPGA, design Shaheen's PCB board and silicon bring-up.

- Contributed to the tape-out of Carfield's SoC (Intel 16nm). Carfield is the first prototype in the advanced Intel16 FinFet technology of the Open-Research platform for safe, resilient, and time predictable systems. Been in charge of the integration, wake-up, and offload of vector workloads to the Spatz cluster.
- Led the tape-out of AlSaqr's SoC (GlobalFoundries 22nm) development. AlSaqr is enhanced by dual 64-bit RV64 Linux-capable cores with cache coherency based on the AXI ACE protocol; it includes a cluster with 8 RV32 cores and a Tensor Unit accelerator. AlSaqr sets a new standard in security by integrating a Secure Subsystem based on the Opentitan project.
- Led the tape-out of Maestro's SoC (TSMC 65nm) development. Maestro features two domains: a 32-bit RISC-V host domain with a single-core Ibex processor and a 64-bit vector domain with Spatz, a compact RISC-V vector processor with an integrated Tensor unit. The vector domain also includes a Floating-Point FFT accelerator, boosting Maestro's performance in frequency domain applications.
- Led the tape-out of Buckbeak's SoC (GlobalFoundries 22nm) development. Buckbeak is an SoC designed for compact and flexible on-demand reconfigurability of a dual-vector core cluster. It features a 32-bit RISC-V host domain with a single-core Ibex processor and a 64-bit reconfigurable vector domain with Spatzformer. Spatzformer operates in two modes: split mode for dual-core vector processing of concurrent tasks and merge mode for single scalar core control of non-vectorizable tasks. This dual-domain architecture ensures efficient and adaptable processing for diverse computational needs.

Website https://www.unibo.it/sitoweb/mattia.sinigaglia5 |

Field of study Semiconductor Engineering, Computer Architecture, Digital Design

01/12/2021 Bologna,, Italy
COMPUTER SCIENCE ENGINEER - SECTION A University of Bologna

01/09/2018 – 21/07/2021 Bologna,, Italy
MASTER'S DEGREE IN COMPUTER SCIENCE ENGINEERING University of Bologna

Design of a fully RISC-V-based microcontroller architecture derived from the PULP platform. The Echoes SoC is tailored for audio applications, featuring an integrated FFT accelerator and the implementation of Time Division Multiplexing (TDM) in the I2S peripheral for digital audio devices.
The design is implemented in TSMC 65nm technology, targeting a maximum frequency of 200MHz SSG at 1.08V

Field of study Computer Science Engineering | **Final grade** 107 |

Thesis Design and implementation of a System-On-Chip for audio applications

01/09/2012 – 24/07/2017 Bologna, Italy
BACHELOR'S DEGREE IN COMPUTER SCIENCE ENGINEERING University of Bologna

Research and development of video streaming over USB and Linux gadget drivers to configure a Zynq-based system as a USB webcam device. The project centered on designing a USB camera system in which an embedded platform, equipped with an FPGA-based camera, is recognized as a USB device by a host PC.
Additionally, the research delved into image acquisition from a USB-connected camera interfaced with an embedded system running a custom-configured Linux operating system. This configuration enabled efficient real-time image capture and processing.
The hardware platform utilized for the study was the Zynq evaluation board, specifically the Zedboard, which provided the computational and interfacing capabilities necessary for prototyping and testing.

Field of study Computer Science Engineering | **Final grade** 90 |

Thesis Image acquisition and processing from USB camera on Zynq platform”

LANGUAGE SKILLS

Mother tongue(s): **ITALIAN**

Other language(s):

	UNDERSTANDING		SPEAKING		WRITING
	Listening	Reading	Spoken production	Spoken interaction	
ENGLISH	B2	B2	B2	B2	B2

Levels: A1 and A2: Basic user; B1 and B2: Independent user; C1 and C2: Proficient user

DIGITAL SKILLS

Git

Digital Design

HDL(SystemVerilog,Vhdl, Verilog) | Modelsim, Cadence, Synopsis Design Compiler, Hspice | Xilinx Vivado/Vitis | Physical Design(Floorplan, Place & Route, Clock Tree Synthesis) using Innovus | Logical desing (Xilinx, ModelSim)

Programming

C | bash | Assembly

Operating System

Windows | Linux | Mac OS

PUBLICATIONS

2024
Spatzformer: An Efficient Reconfigurable Dual-Core RISC-V V Cluster for Mixed Scalar-Vector Workloads

Perotti, Matteo and Raeber, Michele and Sinigaglia, Mattia and Cavalcante, Matheus and Rossi, Davide and Benini, Luca

2024
A Gigabit, DMA-enhanced Open-Source Ethernet Controller for Mixed-Criticality Systems

Liang, C., Ottaviano, A., Benz, T., Sinigaglia, M., Benini, L., Garofalo, A., \& Rossi, D

2024
A RISC-V Heterogeneous SoC for Embedded Devices

L. Valente, M. Sinigaglia, Y Tortorella, D. Rossi, L. Benini

2024
A Heterogeneous RISC-V based SoC for Secure Nano-UAV Navigation

L. Valente, A. Nadalini, A. Veeran, M. Sinigaglia, B. Sa, N. Wistoff, Y. Tortorella, S. Benatti, R. Psiakis, A. Kulmala, B. Mohammad, S. Pinto, D. Palossi, L. Benini, D. Rossi

2023
HULK-V: a Heterogeneous Ultra-low-power Linux capable RISC-V SoC

L. Valente, Y. Tortorella, M. Sinigaglia, G. Tagliavini, A. Capotondi, L. Benini, and D. Rossi

2023
Shaheen: An Open, Secure, and Scalable RV64 SoC for Autonomous Nano-UAVs

L. Valente, A. Veeran, M. Sinigaglia, Y. Tortorella, A. Nadalini, N. Wistoff, B. Sá, A. Garofalo, R. Psiakis, M. Tolba, A. Kulmala, N. Limaye, O. Sinanoglu, S. Pinto, D. Palossi, L. Benini, B. Mohammad, and D. Rossi

2023
ECHOES: a 200 GOPS/W Frequency Domain SoC with FFT Processor and I2S DSP for Flexible Data Acquisition from Microphone Arrays

M. Sinigaglia, L. Bertaccini, L. Valente, A. Garofalo, S. Benatti, L. Benini, F. Conti, and D. Rossi

CONFERENCES AND SEMINARS

04/12/2023 – 15/12/2023 Hsinchu, Taiwan
Taiwan-Europe Semiconductor Short-term Training Program 2023

Completed the course "Cell-based IC Design, Implementation, and Verification" at the Taiwan Semiconductor Research Institute (TSRI), focusing on advanced methodologies for designing, implementing, and verifying integrated circuits.

Link https://www.taiwanembassy.org/uploads/sites/167/2023/09/Poster-and-Information-Taiwan-Europe-Semiconductor-Training-Program-Integrated-Circuit-Design-and-Implementation-Courses.pdf

18/09/2023 – 22/09/2023 Alghero, Sardegna, Italy

Cyber Phisical Systems Summer School

Completed the summer school "Cyber-Physical Systems (CPS) Engineering and Applications", focusing on the design, implementation, and challenges of CPS, including adaptivity, security, and human-centric design, with hands-on experience using industrial and academic tools.

Link https://www.cpsschool.eu/program-2023/

2023 – 2023 Bologna, Italy

Academic English Skills - AcES

Completed the course "Academic English for International Contexts", aimed at developing written and oral communication skills for drafting academic texts and participating in conferences and congresses in international settings. The course focused on written and oral production, with an emphasis on the syntactic and lexical features of academic English.

Link https://centri.unibo.it/cla/en/courses/cla-academics

21/05/2023 – 25/05/2023 Monterey, California, USA

IEEE International Symposium on Circuits and Systems (IEEE ISCAS 2023)

Presented the Echoes chip, highlighting its innovative architecture tailored for audio applications. Echoes integrates a 64-bit RISC-V processor with an FFT accelerator and TDM-enabled I2S interface, demonstrating advanced capabilities for efficient digital audio processing.

Link https://2023.ieee-iscas.org/

Bologna, 21 Dicembre 2024