europass

Yvan Tortorella

[redacted]

ESPERIENZA LAVORATIVA

Digital IC Designer

Eggtronic [18/11/2024 – Attuale]

Città: Modena | **Paese:** Italia

Design di architetture digitali per HW security in sistemi basati su ISA RISC-V.

Visiting Scientist

European Space Research and Technology Centre (ESTEC) [15/01/2024 – 15/06/2024]

Città: Noordwijk | **Paese:** Paesi Bassi

- Project leader in the tape-out of a highly heterogeneous System on Chip (SoC) for space and satellite applications based on the RISC-V Instruction Set Architecture (ISA) in collaboration with Thales Alenia Space.
- Implementation of RISC-V-based multicore computing systems using Ultra-Deep Sub-Micron (UDSM) technologies such as TSMC 7nm.
- Taking part to UDSM activities issued by ESA for defining future generation of european space processors.

University teaching assistant

Alma Mater Studiorum - Università degli studi di Bologna [01/03/2023 – 30/09/2023]

Città: Bologna | **Paese:** Italia

ASIC Designer

PULP Platform [01/11/2021 – 31/10/2024]

Città: Bologna | **Paese:** Italia

- Design of RISC-V-based mixed-critical SoCs for real-time, performance, energy efficient, and reliable computing.
- Design of application-specific hardware accelerators and integration in complex multi-core and many-core systems.
- Tape-out of \href{http://asic.ethz.ch/authors/Yvan_Tortorella.html}{multiple chips} in different technology nodes.
- Contributor and member in the \href{https://www.isolde-project.eu/}{ISOLDE} European project.

ISTRUZIONE E FORMAZIONE

Dottorato di Ricerca

Alma Mater Studiorum - Università degli Studi di Bologna [01/11/2021 – 31/10/2024]

Città: Bologna | **Paese:** Italia | **Campi di studio:** Ingegneria Elettronica | **Tesi:** RISC-V-Based Heterogeneous Computing Platform For Satellite and Space Applications

Laurea Magistrale

Alma Mater Studiorum - Università degli Studi di Bologna [15/09/2018 – 11/10/2021]

Città: Bologna | **Paese:** Italia | **Campi di studio:** Ingegneria Elettronica | **Voto finale:** 110/110 con Lode | **Tesi:** Design of a Low-Precision Floating-Point Matrix Multiplication Accelerator for On-Chip Deep Learning [redacted]

COMPETENZE LINGUISTICHE

Altre lingue:

inglese

ASCOLTO C1 **LETTURA** C1 **SCRITTURA** C1

PRODUZIONE ORALE C1 **INTERAZIONE ORALE** C1

Livelli: A1 e A2: Livello elementare B1 e B2: Livello intermedio C1 e C2: Livello avanzato

COMPETENZE DIGITALI

System verilog / programmazione : linguaggio di programmazione C / Windows e Linux (interfaccia grafica e comandi da shell) / Python & Bash Scripting / Makefile / Versionamento: Git, GitHub / QuestaSim/ModelSim (avanzato) / Synopsis Design Compiler / Cadence Innovus / Xilinx: Vivado, ISE, ISim, EDK, SDK, ChipScope

PROGETTI

[01/09/2023 – 16/09/2024]

Astral

Heterogeneous space platform for reliable computing with runtime-selectable fault tolerance reconfiguration. Result of a collaboration between the University of Bologna and Thales Alenia Space.

Role: System architect and designer.

Link: http://asic.ethz.ch/2024/Astral.html

[01/03/2023 – 11/11/2023]

Carfield

Heterogeneous platform taped out in Intel 16 nm FinFet technology for automotive applications.

Role: system-level co-architect; responsible for the main IPs integration and testing; responsible for the bringup and testing of safety-critical features.

Link: http://asic.ethz.ch/2023/Carfield.html

[01/03/2023 – 01/12/2023]

Maestro

Chip prototyped in TSMC 65 nm technology leveraging a tiny (256-bit) vector processor empowered with tensor computing capability and FFT-dedicated hardware accelerator, thus tailored for acceleration of radar and machine learning workloads.

Role: system-level co-architect; project supervisor.

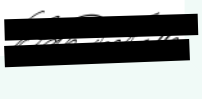
Link: http://asic.ethz.ch/2023/Maestro.html

[01/09/2021 – 01/04/2022]

Shaheen

Heterogeneous Linux-capable SoC prototyped in Global Foundries 22 nm FDSOI technology for autonomous drones navigation.

Role: system-level integration and validation of a multicore software-programmable accelerator; hardware extension to support IO virtual memory management and heterogeneous offloading.



Link: http://asic.ethz.ch/2022/Shaheen.html

[01/01/2021 – 15/07/2021]

Darkside

Chip prototyped in TSMC 65 nm technology tailored for on-chip training and inference of general Deep Learning models.

Role: design, testing, and integration of a tensor processing unit for matrix multiplication execution in FP16/FP8 precision for on-chip training of general Deep Learning models.

Link: http://asic.ethz.ch/2021/Darkside.html

PUBBLICAZIONI

[2023]

Hybrid modular redundancy: Exploring modular redundancy approaches in RISC-V multi-core computing clusters for reliable processing in space

M. Rogenmoser, Y. Tortorella, D. Rossi, F. Conti, L. Benini; ACM Transactions on Cyber-Physical Systems (2023)

[2023]

RedMule: A Mixed-Precision Matrix-Matrix Operation Engine for Flexible and Energy-Efficient On-Chip Linear Algebra and TinyML Training Acceleration

Scrivi qui la descrizione...

Y. Tortorella, L. Bertaccini, L. Benini, D. Rossi, F. Conti; Future Generation Computer Systems, Special Issue on Integration of Machine Learning and Edge Computing for Next Generation of Smart Wearable Systems (2023)

[2023]

PULP Fiction No More—Dependable PULP Systems for Space

M. Ulbricht, Y. Tortorella, M. Rogenmoser, L. Lu, J. Chen, F. Conti, M. Krstic, L. Benini; 2023 IEEE European Test Symposium (ETS)

[2023]

RISC-V Processor Technologies for Aerospace Applications in the ISOLDE Project

W. Fornaciari, F. Reghenzani, G. Agosta, D. Zoni, A. Galimberti, F. Conti, Y. Tortorella, et al.; International Conference on Embedded Computer Systems

[2023]

Shaheen: An Open, Secure, and Scalable RV64 SoC for Autonomous Nano-UAVs

L. Valente, A. Veeran, M. Sinigaglia, Y. Tortorella, et al.; 2023 IEEE Hot Chips 35 Symposium (HCS)

[2022]

RedMulE: A compact FP16 matrix-multiplication accelerator for adaptive deep learning on RISC-V-based ultra-low-power SoCs

Y. Tortorella, L. Bertaccini, D. Rossi, L. Benini, F. Conti; 2022 Design, Automation \& Test in Europe Conference \& Exhibition (DATE)

[2023]

HULK-V: a Heterogeneous Ultra-low-power Linux capable RISC-V SoC

L. Valente, Y. Tortorella, M. Sinigaglia, G. Tagliavini, A. Capotondi, L. Benini, D. Rossi; 2023 Design, Automation \& Test in Europe Conference \& Exhibition (DATE)

[2022]

Darkside: A heterogeneous RISC-V compute cluster for extreme-edge on-chip DNN inference and training

A. Garofalo, Y. Tortorella, M. Perotti, L. Valente, A. Nadalini, L. Benini, D. Rossi, F. Conti; IEEE Open Journal of the Solid-State Circuits Society (2022)

[2022]

Darkside: 2.6 GFLOPS, 8.7 mW heterogeneous RISC-V cluster for extreme-edge on-chip DNN inference and training

A. Garofalo, M. Perotti, L. Valente, Y. Tortorella, A. Nadalini, L. Benini, D. Rossi, F. Conti ;ESSCIRC 2022-IEEE 48th European Solid State Circuits Conference (ESSCIRC)

Autorizzo il trattamento dei miei dati personali presenti nel CV ai sensi dell'art. 13 d. lgs. 30 giugno 2003 n. 196 - "Codice in materia di protezione dei dati personali" e dell'art. 13 GDPR 679/16 - "Regolamento europeo sulla protezione dei dati personali".