

PERSONAL INFORMATION **Millesimo Maurizio**

## WORK EXPERIENCE

September 2022 – on going **Teaching Tutor**

Alma Mater Studiorum-University of Bologna  
Department of Electrical, Electronic, and Information Engineering "Guglielmo Marconi"  
Campus di Cesena, Via Dell'Università 50, Cesena (FC), Italy  
Teaching tutor of the Master Degree course: Electronic Measurements

February 2022 - August 2022 **Internship**

IMEC zvw  
Kapeldreef 75, 3001 Leuven (Belgium)  
Topic: Characterization of buffer traps/defects causing ON-Resistance degradation of GaN-based High Electron Mobility Transistor (HEMT) for power applications. The work was performed on on-wafer devices through the use of Probe Station and Source Measure Unit (SMU). The buffer traps has been characterized by means of Depp-Level Transient Spectroscopy (DLTS) technique on devices featuring different characteristics, such as:

- Carbon doped GaN back barrier thickness;
- Superlattice buffer thickness;
- thickness and Aluminum concentration of the AlGaIn layer;
- AlN nucleation layer thickness;

The variation of these parameters has allowed to understand which layer has the dominant impact on the ON-Resistance degradation mechanisms.

September 2021 – August 2022 **Teaching Tutor**

Alma Mater Studiorum-University of Bologna  
Department of Electrical, Electronic, and Information Engineering "Guglielmo Marconi"  
Campus di Cesena, Via Dell'Università 50, Cesena (FC), Italy  
Teaching tutor of the Master Degree course: Electronics Laboratory for Renewable Energy

April 2020 – October 2020 **Junior Researcher**

Advanced Research Center on Electronic Systems (ARCES) – University of Bologna  
Via Dell'Università 50, Cesena (FC), Italy  
Topic: Experimental Characterization and TCAD modeling of GaN-based High Electron Mobility Transistor (HEMT) with p-GaN gate technology.

September 2019 – March 2020 **Internship**

IMEC zvw  
Kapeldreef 75, 3001 Leuven (Belgium)

Topic: Characterization and reliability study of GaN-based High Electron Mobility Transistor (HEMT) with p-GaN gate technology. The work was performed on on-wafer devices through the use of Probe Station and Source Measure Unit (SMU). Reliability was investigated in the region of OFF-State operation, with the characteristics of the devices varied, such as:

- thickness of AlGaIn and GaN layers;
- Aluminum concentration in the AlGaIn layer;
- distance between gate and drain;
- configuration of field plate lengths.

The variation of these parameters has allowed to understand the degradation mechanisms affecting such devices under OFF-State condition.

## EDUCATION AND TRAINING

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2020–On going

### PhD Fellowship in Electronics, Telecommunications and Information Technologies Engineering

Alma Mater Studiorum-University of Bologna, Campus of Cesena, Cesena (FC), Italy

Research Project Title : "Experimental Characterization and TCAD Modeling of GaN-based Power Devices Reliability"

2017–2020

### Master Degree in Electronics and Telecommunications Engineering for Energy

Alma Mater Studiorum-University of Bologna, Campus of Cesena, Cesena (FC), Italy

Marked 109 points over 110 maximum

Thesis Title : "OFF-State Reliability of pGaN Power HEMTs"

2012–2017

### Bachelor Degree in Electronic Engineer

Università degli Studi della Calabria-UNICAL, Rende (CS), Italy

Thesis Title : "Design and implementation of laboratory instruments with Arduino and LabVIEW".

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**PERSONAL SKILLS**

Mother tongue Italian

## Other languages

	UNDERSTANDING		SPEAKING		WRITING
	Listening	Reading	Spoken interaction	Spoken production	
English	B2	B2	B2	B2	B2
Spanish	B1	B1	B1	B1	B1

Levels: A1 and A2: Basic user – B1 and B2: Independent user – C1 and C2: Proficient user  
[Common European Framework of Reference for Languages](#)

**Technical skills**

- Very good knowledge of Microsoft applications and Office package, especially Excel, Word, PowerPoint.
- Known programming languages: Java, C/C++, VHDL, Matlab (certificate from the online training courses in Fundamentals, Programming Techniques and Machine Learning) and Simulink.
- Excellent knowledge of softwares: Sentaurus TCAD, OriginLab, LabVIEW, Xilinx, DIALux, KiCAD, ElectricVLSI (Integrated Circuit Design).
- Experience using electronic instrumentation, particularly Probe Station, Source Measure Unit, LCR-meter, Waveform Generator, digital memory oscilloscopes, multimeters, function generators, power supplies, breadboards for prototyping electrical circuits.
- Extensive experience in experimental setups and types of tests aimed at characterization and reliability studies of semiconductor devices for power electronics applications.
- Extensive experience in experimental data processing;
- Extensive knowledge of physical and mathematical models for performance/reliability degradation mechanisms of semiconductor-based devices;
- Extensive knowledge of architectures and related issues of power converters.
- Excellent internet browsing and research skills.

**Organisational and communication skills**

- Good general culture assimilated during the years of study.
- Strong predisposition to interpersonal relationships, sociable, open to learning and team activities.
- Wide ability to adapt and deal with new realities, ability to adapt to multicultural environments.
- Seriousness, dynamism, stubbornness, determination, flexibility and immense passion for technologies.

Driving licence A, B

**PUBLICATIONS**

- [1] M. Millesimo; M. Borga; B. Bakeroot; ; N. Posthuma; S. Decoutere; E. Sangiorgi; C. Fiegna; A. N. Tallarico. "The Role of Frequency and Duty Cycle on the Gate Reliability of p-GaN HEMTs". In: *IEEE Electron Device Letter* (May 2022).
- [2] M. Millesimo; B. Bakeroot; M. Borga; N. Posthuma; S. Decoutere; E. Sangiorgi; C. Fiegna; A. N. Tallarico. "Gate Reliability of p-GaN Power HEMTs Under Pulsed Stress Condition ". In: *2022 IEEE International Reliability Physics Symposium Proceedings (IRPS), Dallas(TX, USA)* (March 2022).
- [3] A.N. Tallarico; M. Millesimo; B. Bakeroot; M. Borga; N. Posthuma; S. Decoutere; E. Sangiorgi; C. Fiegna. "TCAD Modeling of the Dynamic VTH Hysteresis under Fast Sweeping Characterization in p-GaN Gate HEMTs". In: *IEEE Transactions on Electron Devices (Accepted)* (2021).
- [4] M. Millesimo; A.N. Tallarico; N. Posthuma; M. Borga; B. Bakeroot; S. Decoutere; C. Fiegna. "High-Temperature Time-Dependent Gate Breakdown of p-GaN HEMTs". In: *IEEE Transactions on Electron Devices, vol. 68, no. 11, pp. 5701-5706* (November 2021).

- [5] M. Millesimo; N. Posthuma; B. Bakeroot; M. Borga; S. Decoutere; A. N. Tallarico. "Impact of Structural and Process Variations on the Time-Dependent OFF-State Breakdown of p-GaN Power HEMTs." In: *IEEE Transactions on Device and Materials Reliability*, vol. 21, no. 1, pp. 57-63 (March 2021).