Alessandro Piovaccari

Chief Scientist, Lifetime Fellow, Former CTO/SVP, Semiconductors Enthusiast

5 Wren Valley Cv, West Lake Hills, TX 78746
[redacted]

Summary

- 30 years of professional experience in the field of semiconductors and IC design
- 5 years of professional experience in the field of AI/ML
- Successful track record in leading projects developing innovative products, from concept to market delivery
- Direct technical and management contribution to products with an overall greater than 4-billion unit shipment
- Broad experience working with leading customers, and marketing and engineering teams on roadmap definition
- Deep understanding of semiconductor products life cycle: definition, architecture, design, manufacturing, integration, sales, and aftermarket services
- Extensive experience working with foundries on process definition, EDA companies on tools improvements
- Solid IC design know-how: device physics, analog & RF design, wireless & IoT mixed-signal SoC, embedded systems, edge security, edge AI/ML
- Good knowledge in embedded SW development, quality assurance, and release process
- Big promoter of HW-SW co-design and using regression verification methodologies in both digital and analog design
- Advocate and pioneer on the use of AI/ML and open-source RISC-V in ultra-low-power embedded products
- Successful leader and team player that leverages technology and teamwork for solving real-world problems
- Good experience managing HW & SW multi-cultural engineering teams across multiple design centers and continents
- Recognized for building strong teams, organizations between key members within the semiconductor community
- Extensive network within the semiconductor community, both industry and academia

Work Experience

Circuit AI, Austin, TX — *July 2024 – Present*

Chief Scientist

- Revolutionizing Knowledge: Turn Everyday Information into Extraordinary Insights

Alma Mater Studiorum – Università di Bologna, Italy — *July 2021 – Present*

Adjunct Professor, *AA 2022-2023, AA 2023-2024*

- Electronic Frontiers M (IC Design at the Edge of Moore's Law) – MSEE core course

Visiting Fellow, *July 2021 – June 2022, September 2022 – August 2024*

- Fellowship in approaches, methods, and practices in integrated circuit design in leading fabless companies
- Lecturing on semiconductor technology and industry at the ETIT Ph.D. School

Università di Pavia, Italy — *April 2024 – Present*

Visiting Professor, *AA 2023-2024*

- Device Physics for IC Designers (Physical Architecture Design) - MSEE /PhD elective course

Apicio Enterprises LLC – Austin, TX *July 2021 – Present*

Principal CEO/CTO

- Semiconductors consulting services – analog/mixed-signal & RF SoC design, process technology, IC manufacturing, roadmaps and product strategy, R&D organization [*More information available upon request*]

Silicon Labs, Austin, TX (NASDAQ:SLAB) *November 2003 – June 2021*

Lifetime Fellow, *May 2021*

- First Lifetime Fellow in the company

CTO & SVP of Central R&D, *October 2019 – April 2021*

- Company's central engineering and the advanced R&D departments
- Next-gen SoCs HW/SW architectures and IP - RISC-V, edge AI/ML and security cores - advanced process nodes - EDA tools and cloud computing
- M&A technical due diligence and engineering team integration
- Managed a worldwide team of about 140 engineers: multiple design centers across 3 continents (NA, EU, AP)

CTO & SVP of Engineering, *February 2015 – September 2019*

- Company's product and technology R&D, including both hardware and software engineering
- Low-power Wi-Fi incubator - First low-power Wi-Fi radio officially supported in the Linux kernel
- M&A technical due diligence and engineering team integration
- Managed a worldwide team of more than 300 engineers: 9 design centers across 4 continents (NA, EU, AP and Oceania)

VP of Engineering, Broadcast & IoT, *February 2013 – January 2015*

- IC design engineering R&D for MCUs (8/32-bit), Wireless SoCs (802.15.4, ZigBee, BLE and Sub-GHz), and broadcast audio and video products
- IoT M&A technical due diligence and engineering team integration
- Managed team of about 90 analog and digital designers: 4 design centers across 2 continents (NA, EU)

Director of Engineering, Broadcast Video and Wireless, *February 2011 – January 2013*

- IC design engineering for wireless SoCs (802.15.4, ZigBee) standards, and broadcast video products
- Managed team of about 60 analog and digital designers: 5 design centers in 2 continents (NA, EU)

Design Engineering Manager, Broadcast Video, *October 2006 – January 2011*

- Leader and co-architect of the first single-chip worldwide TV tuner
- Ultra-thin flat-screen TV enabler
- More than 2B units shipped - Still in production (Skyworks) with 90% market share and adopted by 9 of the top 10 TV manufacturers
- Built and managed an Analog/RF team of 15 engineers

Sr. Design Engineering, Broadcast Audio, *November 2003 – September 2006*

- First hire and major contributor to the single-chip AM/FM tuner / transmitters
- Almost 2B units shipped - Still in production (Skyworks) - Employed by major manufacturers in iconic products

Cadence Design Systems (NASDAQ:CDNS) *October 1998 – October 2003*

Sr. Service Manager – Cary, NC Design Center, *July 2001 – October 2003*

- Technical manager of an engineering team of 25
- Development and support of SerDes IP in various sub-micron CMOS technologies
- The SerDes IP have been used in many mainstream products including workstations networking and chip-to-chip links (CPU-GPU) in game consoles

Principal Engineer – Columbia, MD Design Center, *October 1998 – June 2001*

- RFIC and PMIC design engineer (LNAs, RF PAs, LOG amps, RSSI detectors, LDOs, high-speed DACs) for wireless (DECT, Bluetooth, AMPS) and cable products

- The DECT/BT RFIC was used in very popular cordless phone, in mass production for decades The PA was probably one of the first fully-integrated CMOS PA in a commercially available RFIC

Tanner Research – Pasadena, CA *February 1997 – September 1998*

(Acquired by Mentor Graphics, now Siemens EDA)

Research Scientist

- R&D on the field of CMOS neuromorphic image sensors and processor
- Developed an analog image motion processor based on 2D wave propagation for satellite applications
- Developed an analog sea-of-gates methodology for fast prototyping of baseband analog ICs, with quick manufacturing turnaround, which was subsequently granted a significant US government grant

Università di Bologna – Bologna, Italy *July 1993 – January 1997*

Design Engineering Consultant

- Developed a BiCMOS AFE IC for an amorphous silicon X-Ray imager
- Developed a BiCMOS AM/FM RFIC short antennas preamplifier for automotive applications
- Developed a fully-integrated CMOS muscle electro-stimulator IC for rehabilitation therapy devices

Boards, Advisory Boards, and Executive Committees

Lynceus – Paris, France *August 2022 – Present*

Advisory Board Member, Strategy Consultant

- AI-powered end-to-end automation for semiconductors manufacturing and metrology

Cormint Data Systems – Fort Stockton, TX *April 2022 – Present*

Technical Advisor

- Building the strongest electricity grid in the world, backed by Bitcoin mining

Silicon Catalyst – San Francisco, CA *September 2021 – Present*

Advisor

- The world's only incubator which accelerates startups focused on semiconductor solutions

Berkeley Skydeck – Berkeley, CA *September 2021 – Present*

Chip Track Advisor

- High-tech entrepreneurship startup accelerator and incubator program

Johns-Hopkins University – Baltimore, MD *December 2018 – Present*

Advisory Board Member, Center for Leadership Education (CLE)

- Develop influential and imaginative leaders by preparing students across the university to translate their innovations from the classroom and lab to the real world and to effectively transition from academic to professional life

University of Texas at Austin – Austin, TX *November 2018 – Present*

Advisory Council Member, UTeach, College of Natural Sciences

- Create lifelong STEM educators fostering our nation's secondary students' educational success

Skillpoint Alliance – Austin, TX *September 2015 – Present*

Board Director

- Provide a gateway for individuals to transform their lives through rigorous skills-based training and education

Driver AI – Austin, TX *February 2024 – August 2024*

Advisory Board Member, Strategy Consultant

- AI/LLM powered design and decision-making interpreter tool for technology stacks

Energous Corporation – San Jose, CA (NASDAQ:WATT) *May 2022 – May 2024*

Advisory Board Member

- Certified wireless power charging-at-a-distance technology

Diakopto – San Jose, CA *May 2022 – June 2023*

(Acquired by Ansys in Jun 2023, which is currently being acquired by Synopsys)

Advisory Board Member

- EDA tools to enable IC engineers designing next-generation ICs

OpenHW Group – Ottawa, ON, Canada *June 2019 – May 2021*

Founding Member, Board Director

- Drove the team responsible to bring the CV32E40P (PULP RI5CY) RISC-V core to industrial-strength verification level

Technology Councils and Technical Committees

IEEE Solid-State Circuits Society (SSCS) *January 2020 – Present*

Vice President of Conferences, AdCom Member, *January 2022 – Present*

- Supervisor of all the SSCS financially sponsored conferences: ISSCC, CICC, VLSI, ESSCIRC and A-SSCC

Founder and Chair, Chiplets Solutions for IC Designers Workshop (CHISIC), *December 2023 – Present*

- First SSCS chiplets event focused to IC designers. Now a permanent event.

Vice Chair, Central Texas SSCS/CAS Joint Chapter, *January 2020 – Present*

- Promote the diffusion of leading-edge IC design knowledge within the local Central Texas community

Global Semiconductor Alliance (GSA) *September 2018 – Present*

CTO Council Member

- Forum for CTOs from leading semiconductor companies to meet and discuss technology trends, opportunities, challenges, best practices, and solutions

IEEE Conference on AgriFood Electronics (CAFE) *July 2023 – Present*

Steering Committee Member, *September 2023 – Present*

- Conference planning, organization and direction

Organization Committee Member, *July 2023 – September 2023*

- SSCS Special Sessions Chair 2023

IEEE Custom Integrated Circuits. Conference (CICC) *April 2022 – February 2009*

Steering Committee Member

- Chair positions: TPC 2017, Conference 2018, Genera 2019, Strategic Development 2020-2022
- Conference fundamental re-org 2017 - First SSCS virtual conference 2020

Technical Program Committee (TPC) Member

- Chair positions: Analog Techniques 2013-2014 - Sponsorship 2014

Forbes Technology Council *September 2018 – September 2022*

Technology Council Member

- Organization comprised of leading CIOs, CTOs and technology executives.

Education

Johns-Hopkins University – Baltimore, MD

Advanced Post-Master, EECS – *May 2002*

- GPA: 4.0 Summa Cum Laude
- Focus: RF and microwave design
- Final research project: Harmonic Balance simulator in Matlab for microwave applications

Università di Bologna – Bologna, Italy

PhD, EECS – *June 1998*

- Focus: low-voltage low-power analog CMOS design and neuromorphic vision processors.
- Thesis: Low-Voltage Low-Power CMOS Analog Circuits

MS (Laurea), EECS – *May 1993*

- Final score: 100/100
- Focus: Analog Circuits Design, Quantum Electronics, IC Manufacturing, Parallel Computer Architectures
- Thesis: Low voltage and low-power CMOS analog design (Building Blocks for Cellular Neural Networks)

Honors and Awards

- Silicon Labs Lifetime Fellow
- IEEE Solid-State Circuits Society (SSCS) special recognition for leadership on the organization of the first SSCS virtual conference during pandemic (CICC 2020)
- Silicon Labs Patent of the Year
- Johns-Hopkins University Summa Cum Laude graduate

Technical Skills

- *EE areas of expertise*: good knowledge of analog and digital circuit design, especial RF and data converters; device physics and microelectronics manufacturing process
- *Fundamental skills*: quantum mechanics; information theory; Fourier and harmonic analysis; approximation theory.
- *Programming languages*: proficient in Python, Julia, Matlab and Mathematica; good knowledge of C, JavaScript, Node.jS, Lisp, Fortran, and various markup languages; some knowledge of C++
- *CAD EDA tools*: Cadence and Mentor tools. Great proficiency on methodology and design flow automation
- *Spoken languages*: fluency in English and Italian; intermediate proficiency in Spanish, French; some knowledge of Norwegian; elementary knowledge of Korean

Other Activities

- Outdoor sports and activities (hiking, mountain biking, road biking, off-road trials motorcycles, alpine skiing)
- Collector of old and antique scientific and engineering books
- Collector of classic HP calculators

US Patents

- 10,044,383 Sinewave generation from multi-phase signals
- 9,979,404 Multi-phase amplitude and phase modulation

- 9,800,281 Signal processor suitable for low intermediate frequency (LIF) or zero intermediate frequency (ZIF) operation
- 9,647,623 Signal processor suitable for low intermediate frequency (LIF) or zero intermediate frequency (ZIF) operation
- 9,491,394 Configurable buffer for an integrated circuit
- 9,219,512 Integrated receiver and integrated circuit having integrated inductors and method therefor
- 9,036,091 Receiver and method of receiving analog and digital television signals
- 8,983,419 Integrated receiver and integrated circuit having integrated inductors and method therefor
- 8,880,018 Rotating harmonic rejection mixer
- 8,874,060 Radio frequency (RF) receiver with frequency planning and method therefor
- 8,848,110 Mixed-mode receiver circuit including digital gain control
- 8,781,428 Frequency synthesizer
- 8,774,750 Method and apparatus for controlling a harmonic rejection mixer
- 8,768,281 Method and apparatus for controlling a harmonic rejection mixer
- 8,749,417 Multi-mode analog-to-digital converter
- 8,729,925 Configurable buffer for an integrated circuit
- 8,725,099 Rotating harmonic rejection mixer
- 8,706,069 Integrated receivers and integrated circuit having integrated inductors
- 8,587,398 Shielded differential inductor
- 8,543,077 Method and apparatus for controlling a harmonic rejection mixer
- 8,521,099 Transceiver having multiple signal processing modes of operation
- 8,503,962 Implementing a rotating harmonic rejection mixer (RHRM) for a TV tuner in an integrated circuit
- 8,494,470 Integrated receivers and integrated circuit having integrated inductors
- 8,428,536 Low-cost receiver using automatic gain control
- 8,385,867 Tracking filter for a television tuner
- 8,320,863 Rotating harmonic rejection mixer
- 8,264,387 Transceiver having multiple signal processing modes of operation
- 8,260,244 Rotating harmonic rejection mixer
- 8,145,172 Low-cost receiver using tracking filter
- 8,145,170 Low-cost receiver using tracking bandpass filter and lowpass filter
- 8,126,420 Correcting for phase noise of an oscillator
- 8,032,090 Antenna for use in portable applications
- 7,928,878 Analog to digital converter with low out of band peaking
- 7,860,480 Method and apparatus for controlling a harmonic rejection mixer
- 7,756,504 Rotating harmonic rejection mixer
- 7,426,376 Receiver having digital automatic gain control
- 7,321,324 Unconditionally stable analog-to-digital converter
- 6,229,289 Power converter mode transitioning method and apparatus

Peer-Reviewed Publications

- A. Rafi, A. Piovaccari, P. Vancorenland and T. Tuttle, "A harmonic rejection mixer robust to RF device mismatches," *2011 IEEE International Solid-State Circuits Conference*, San Francisco, CA, 2011, pp. 66-68. [67 citations]
- Y. Jiang and A. Piovaccari, "A compact phase interpolator for 3.125G Serdes application," *Southwest Symposium on Mixed-Signal Design, 2003*, 2003, pp. 249-252. [20 citations]
- G. Levy and A. Piovaccari, "A CMOS low-power, high-speed, asynchronous comparator for synchronous rectification applications," *2000 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2000, pp. 541-544 vol.2. [16 citations]
- S. Graffi, G. Masetti, A. Piovaccari, “Criteria to reduce failures induced from conveyed electromagnetic interferences on CMOS operational amplifiers,” *Microelectronics Reliability*, Volume 37, Issue 1, 1997, Pages 95-113. [29 citations]

- A. Piovaccari, "CMOS integrated third-generation current conveyor," *Electronic Letters*, Volume 31, Issue 15, 20 July 1995, p. 1228 – 1229. [65 citations]
- M. Tartagni, A. Piovaccari, F. Vuoto, G. Masetti, "MOST-only normalization module for position-sensitive devices," *Electronic Letters*, Volume 31, Issue 7, March 1995, p. 514 – 515. [1 citation]
- A. Piovaccari, G. Setti, "A versatile CMOS building block for fully analogically-programmable VLSI cellular neural networks," *Proceedings of the Third IEEE International Workshop on Cellular Neural Networks and their Applications (CNNA-94)*, 1994, pp. 347. [2 citations]

Other Publications

- A. Piovaccari, "Optimist's Take: How Technology Can Reshape Post-Pandemic World," *EETimes*, 29 May 2020.
- A. Piovaccari, "The Art and Science of RF and Mixed Signal Design," *Embedded Computing Design*, 10 November 2014.

Keynotes

- "I Chip e la Vita Quotidiana – Un Romagnolo nella Silicon Valley," Keynote & Panel, *Rotary Forlì Tre Valli, Circolo Aurora*. Forlì (Italy): 6 April 2022.
- "IoT End-node: Built to Last," Conference Keynote, *2021 International Reliability Physics Symposium (IRPS 2021)*. Dallas, TX: March 2021. (Virtual Event)
- "The SoC-larity is near!" Opening Keynote, *Kickoff Event for the Georgia Tech Center of Circuits and Systems (CCS)*, Atlanta, GA, 28 January 2021. (Virtual Event)
- "Make of the IoT: Engineering without Borders," Opening Keynote, *MakeCU*, Columbia University, 24 February 2018.

Courses, Lectures and Seminars

- "The Semiconductor Ecosystem," *ET-IT Ph.D. School Seminar*, University of Bologna. Bologna (Italy): 23 July 2024.
- "An Introduction to the Semiconductor Industry," *ET-IT Ph.D. School Seminar*, University of Bologna. Bologna (Italy): 16 July 2024.
- "Sensing, Sampling, Quantization, and Information Theory – A Practical Approach," *LASCAS Tutorial IV*. Punta del Este, (Uruguay): 27 February 2024.
- "Electronic Frontiers M," MSEE course, *Alma Mater Studiorum – Università di Bologna*. Bologna (Italy): AA 2023-24.
- "Device Physics for IC Designers (Physical Architecture Design)," MSEE and Ph.D. course, *Università di Pavia*. Pavia (Italy): AA 2023-24.
- "Electronic Frontiers M," MSEE course, *Alma Mater Studiorum – Università di Bologna*. Bologna (Italy): AA 2022-23.
- "Fundamentals of Sensing, Sampling and Quantization," *ISCAS Short Course*. Austin, TX: 29 May 2022.
- "The Semiconductor Crisis: A Wide but Personal Perspective," *Seminar*, ETH Zürich. Zürich (CH): 12 April 2022.
- "An Introduction to the Semiconductor Industry," *ET-IT Ph.D. School Short Course,* University of Bologna. Bologna (Italy): 25 March, 1 and 8 April 2022.
- "The Semiconductor Crisis: A wide but personal (and maybe oversimplified) perspective," University of Bologna. Cesena (Italy): 21 December 2021.
- "Cross-functional IC Design for the IoT Era," *TxACE*, University of Texas at Dallas. Dallas, TX: 16 October 2017.
- "The IoT Node: The Wireless Superhero," *DAC 2017, Radios for the Next 50 Billion Devices*. Austin, TX: 20 June 2017.
- "The IoT Re-evolution: Opportunities and Challenges for the Design Engineering Community," *Stanford Talks*, Stanford University. Palo Alto, CA: 28 January 2016.
- "The IoT in 2020: The Energy Consumption Dilemma," *CTO Forum*. San Francisco, CA: 6 November 2015.
- "A Simple Method to Calculate the Power Spectrum of Distorted Wide-Band Signals," *ECE Colloquium (ECE 500)*, University of Illinois Urbana-Champaign (UIUC). Urbana-Champaign, IL: 12 February 2015.
- "Silicon Labs TV Tuner History," *ECE Colloquium (ECE 500)*, University of Illinois Urbana-Champaign (UIUC). Urbana-Champaign, IL: 12 February 2015.
- "A Simple Method to Calculate the Power Spectrum of Distorted Wide-Band Signals", *Electrical Engineering Seminar Series*, Columbia University. New York, NY: 14 March 2014.

Forums and Panels

- "Where is the balance between circuit and system-level innovation in our solid-state circuit conference?" Panel, *CICC 2023*, San Antonio, TX, 26 April 2023.
- "The future of open-source chip design," Panel Moderator, Circuits Workshop 2 - The Emerging Ecosystem of Open-Source Chip Design, *VLSI Symposium 2022*, Honolulu, HI, 16 June 2022.
- "Internet of Things (IoT)," Panel, *University of Texas ECE Friday Feature Panel*, Austin, TX, 9 April 2021. (Virtual Event)
- "The Semiconductor Industry at a Tipping Point: What's Next?," Panel, *VLSI 2019*, Kyoto, Japan, 10 June 2019.
- "The Internet of Things (IoT)-Back to the Future or No Future?," Lunchtime Panel Session, *RFIC 2019*, Boston, MA, 3 June 2019.
- "Class of 2025: Where Will Be the Best Jobs?," Panel, *2016 IEEE ISSCC*, San Francisco, CA, 1 February 2016.

Media Interviews

- "RISC-V Summit: Silicon Labs Q&A on IoT Hardware," by Brian Buntz, *IoT World Today*, 12 December 12, 2019.
- "RISC-V Grows Globally as an Alternative to Arm and its License Fees," by Dean Takahashi, *Venture Beat*, 11 December 2019.
- "This Expert Says Semiconductor Technology Will Require A New Breed Of 'Renaissance' Engineer," by Forbes Councils Staff, *Forbes*, 6 September 2019.
- "RISC-V Moving Beyond Academia, New Group offers Hardened SoCs," by Nitin Dahad, *EETimes*, 14 June 2019.
- "Brainstorm: The Most and Least Useful Courses for Engineers," by ECN Staff, *EE World*, 3 October 2018.
- "Putting on the Squeeze," by Graham Pitcher, New Electronics, 28 April 2015.
- "Moore's Law at 50," by Ian Poole, *Radio Electronics*, 19 April 2015.
- "The sexy R&D behind boring chip companies," by Ari Levy, 8 August 2014.

Press Releases

- "Energous Corporation Reports 2022 First-Quarter Results," Energous Press Release, *Associate Press*, 11 May 2022.
- "Energous Adds Three Industry Veterans to Board of Advisors as Company Focuses on Powering the Growing Industrial and Retail Internet of Things Ecosystem," Energous Press Release, *BusinessWire*, 2 May 2022.
- "Silicon Labs Appoints Daniel Cooley as Chief Technology Officer – Former CTO Alessandro Piovaccari to Serve as Technical Advisor," Silicon Labs Press Release, *Nasdaq.com*, 23 April 2021.
- "Arm Enables Custom Instructions for Embedded CPUs," ARM Press Release, *BusinessWire*, 8 October 2019.
- "OpenHW Group Created and Announces CORE-V Family of Open-source Cores for Use in High Volume Production SoCs," OpenHW Group Press Release, *PRNewswire*, 6 June 2019.

References

- **Tyson Tuttle** – Circuit AI CEO; Former Silicon Labs' CEO; Board Director, Federal Reserve Bank of Dallas: https://www.linkedin.com/in/tuttle/
- **Kenneth O** – Texas Instruments Distinguished University Chair Professor, EE, University of Texas at Dallas: https://profiles.utdallas.edu/k.k.o
- **Alberto Sangiovanni-Vincentelli** – The Edgar L. and Harold H. Buttner Chair Professor, EECS, UC Berkeley; Co-founder, CTA and Member of the Board of Directors of Cadence Design Systems: https://www.linkedin.com/in/alberto-sangiovanni-vincentelli-5684a/
- **Nav Sooch** – Chairman and Co-founder of Silicon Labs: https://www.linkedin.com/in/nav-sooch-a6910046/
- **Daniel Artusi** – Former CEO of Lantiq, Conexant and Silicon Labs; Board Director of many tech and semi companies: https://www.linkedin.com/in/dan-artusi-2653b55/
- **Thomas Barber** – VP, Communications Infrastructure and Datacenter at Globalfoundries: https://www.linkedin.com/in/thbarber/
- **Sebastian Ahmed** – Silicon Architect, Qualcomm: https://www.linkedin.com/in/sebastianahmed/
- **Marco Tartagni** – Full professor, Alma Mater Studiorum–University of Bologna, Italy; Inventor of the silicon fingerprint sensor: https://www.linkedin.com/in/marcotartagni/

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- **Ramin Poorfard** – VP of Technology, Silicon Labs: https://www.linkedin.com/in/ramin-poorfard-0388331/
- **Eric Naviaski** – Former Fellow and VP of Engineering of Cadence Design Systems: https://www.linkedin.com/in/eric-naviasky-355baa/
- **Geir Førre** – Founder and Former CEO of Chipcom and Energy Micro; Chair of multiple technology startup: https://www.linkedin.com/in/geir-f%C3%B8rre-03785b5/
- **Steven Garret** – Partner at Boulette Golden & Marin L.L.P.; CommUnityCare Board Directors; Formerly Board Director, Chair-elect, Skillpoint Alliance: https://www.linkedin.com/in/stevengarrett/
- **Pam Sheff** – Director at Center for Leadership Education, G.W. Whiting School, Johns Hopkins University: https://www.linkedin.com/in/pam-sheff-65a71915/